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COMPREHENSIVE PHYSICAL MODELING OF NMOSFET HOT-CARRIER-INDUCED DEGRADATION

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Abstract: The role of hot-carrier-induced interface states in NMOSFETs is discussed. A new model is proposed based on measurements in several 0.7μm CMOS technologies of different suppliers. Our model for the first time enables accurate interface state prediction over many orders of magnitude in time for all stress conditions under pinch-off and incorporates saturation. It can easily be implemented in a reliability circuit simulator, enabling more accurate NMOSFET parameter degradation calculations (e.g. ΔI_D, Δg_m etc.).

INTRODUCTION

In recent years, a massive amount of work on NMOSFET hot-carrier degradation has appeared in the literature. Most of this work relied on empirical degradation modeling, using curve fitting to a simple power law to describe the MOSFET parameters' time dependence [1,2]. Some attempts were made to model the actual (physical) damage mechanisms involved [2,3,4]. Focus has been on modeling interface states creation, since NMOSFET hot-carrier degradation is governed by this mechanism. Woltjer [4] described a formulation which is suitable to be implemented in a reliability circuit simulator. Yet, this formulation is still based on a simple power law relationship (*i.e.* $\Delta N_{it} \propto t^n$), where the value "$n$" was averaged over experimentally determined values. Recently, it was noted [5] that n can show smaller values than reported in the literature. Moreover, initial variation in n and eventually saturation effects give rise to problems in modeling DC and AC degradation [6].

NMOSFET DEGRADATION MECHANISMS

Damage to NMOSFETs is usually divided in three distinct effects, the main one being (acceptor type) interface state generation. Second, negative (fixed) charge trapping at higher gate biases and third, but less prominently, the creation of positive charge under low gate voltage conditions. The latter may anneal (recombine) again by subsequent hot-electron injection. However, some positive charge may remain present [7]. The positive fixed charge may be observed in accelerated stresses. However, it shows a very steep fall-off with drain stress bias due to the higher oxide potential barrier for holes. The latter is the reason that hole trapping is less relevant at standard operating conditions.

The construction of the drain can have a paramount effect on the degradation. For LDD

type drains, it is known that interface state generation in the LDD causes increased series resistance and consequently gives rise to altered electric fields in the MOS device [8]. Furthermore, the spacer oxide can be very sensitive to hot-carrier injection, due to its lower quality. If positioned just above the point of injection, it may easily trap (fixed or interface) charges and affect device behavior.

EXPERIMENTAL

Considering the generation of interface states at the Si-SiO_2 interface in the channel and in the LDD, we observed a pronounced saturation of interface state creation for all our experiments. We used LDD as well as conventional drain type NMOSFETs in several 0.7μm CMOS technologies (oxide thickness t_{ox}=15nm) of two different suppliers. Effective channel lengths varied between 0.5-0.8μm and various stress conditions were applied with stress times ranging from 10^{-3} to 10^{5} s. We performed charge pumping (CP) [9] and I-V characterization after stress and observed that the value of n continues to decrease with increasing stress (Figure 1). We believe that the build-up of negative charge in interface states is retarded by Coulomb repulsion of this charge.

MODEL FOR INTERFACE STATES CREATION INCLUDING SATURATION

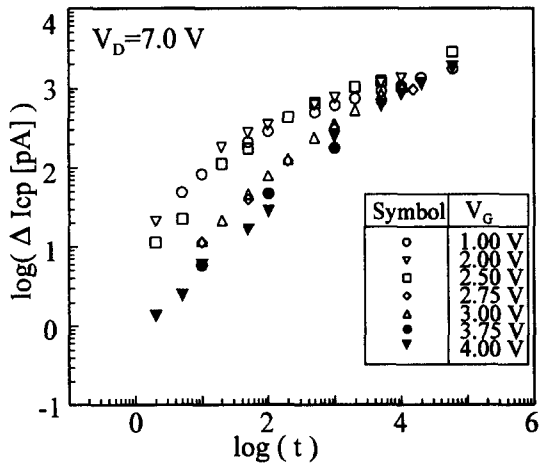

Figure 1. Data of conventional drain NMOSFETs (W=10μm) for different gate stress voltages. Charge pumping conditions: f_{cp}=500kHz, ΔV=4V, V_{rev}=0V, t_{rise}=t_{fall}=100ns (hence, t=τ_{Icp} at ΔI_{cp}=100pA/Hz/m*f_{cp}*W).

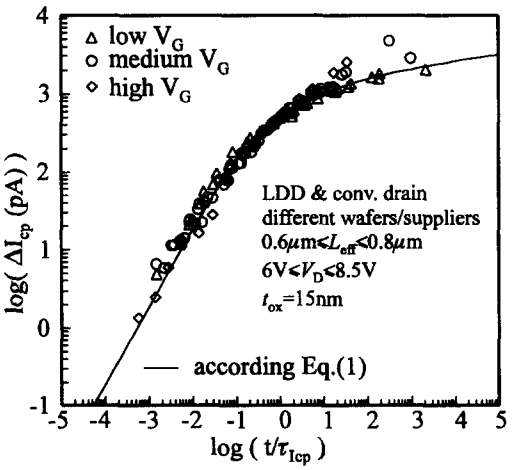

Figure 2. Data of two different suppliers for conventional and LDD NMOSFETs (W=10μm) plotted in one graph. Charge pumping conditions: f_{cp}=500kHz, ΔV=4V, V_{rev}=0V, t_{rise}=t_{fall}=100ns.

Our measured generation of interface states (by means of the net CP current increase ΔI_{cp}) in many hot-carrier experiments for stress conditions under pinch-off and for both LDD as well as conventional drain NMOSFETs, obey one single relation (see Figure 2) given by Eq.(1).

$$\Delta I_{cp}=A.ln(1+C.t/\tau_{Icp}) \quad (1)$$

In Eq.(1), τ_{Icp} is the lifetime at -in our case- a criterion of ΔI_{cp}=100pA/Hz/m. Our model is able to describe the time behavior of the interface state generation and is essentially different from

that of Kim *et al.* [10]. It model enables us to predict interface state generation in NMOSFETs for different bias conditions and geometries, based upon two (constant) parameters A=229pA and C=8.14, which hold for all our experiments so far. The measured ΔI_{cp} falls on one single curve over many orders of magnitude in t/τ_{Icp} for various stress biases under pinch-off. Medium V_G has been defined as $V_G@I_{B,max}\pm 1V$. Measured τ_{Icp} was used in constructing the plot of Figure 2.

Note that the self-limiting behavior is included self-consistently and therefore the model can simultaneously account for the reported varying value of n with stress time [5].

Using the lifetime model given by Eq.(2) as proposed in [4], with one technology-related constant C_w and universal coefficients a and b, we are able to predict τ_{Icp}, (shown in Figure 3).

$$log(\tau_{Icp})=a.[-\phi_{ox}/\phi_i.\log(I_B/I_S)]^b-log(I_S/W)+E_{ox}/E_0-C_{w3} \quad (2)$$

where I_S, I_B, are source and substrate currents respectively, W is transistor width and $\phi_{ox}\approx 3.2eV$, $\phi_i\approx 1.3eV$, $E_{ox}=(V_G-V_T-V_D)/t_{ox}$, $E_0=80MV/m$, $a\approx 11$, $b\approx 0.5$. It must be emphasized here, that choosing another lifetime criterion (*e.g.* 10% transconductance change) will only affect the value of C_w (also shown in Figure 4). Since transconductance shift also contains the effects of fixed charge trapping under accelerated stresses, plotting the quantity τ_{gm} will in general be less accurate, as is observed in the plot.

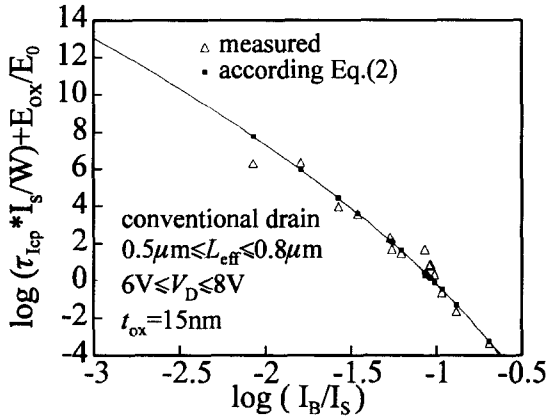

Figure 3. Lifetime plot with oxide field correction [3]. Shown are data from measurement and corresponding data calculated using Eq.(2) for conventional drain NMOSFETs. I_B, I_S are the bulk respectively source current, and $\tau_{Icp}=t@\Delta I_{cp}=100pA/Hz/m$.

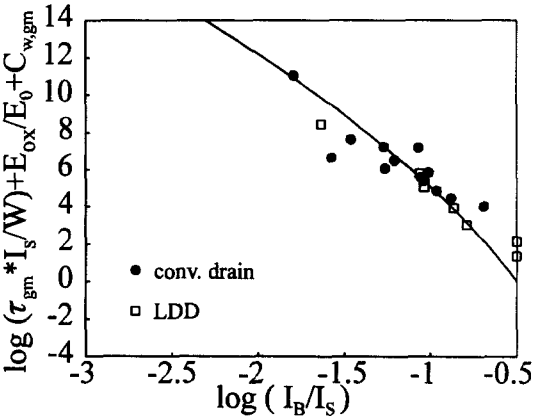

Figure 4. Similar plot as in Figure 3, but now lifetime has been defined as the time where $\Delta g_m=10\%$. Use has been made of the values of $C_{w,gm}$, in Eq.(2) for conventional drain as well as LDD NMOSFETs.

Furthermore, using Eq.(2) to calculate lifetimes τ_{Icp} and substituting this into Eq.(1), we are also able to calculate ΔI_{cp} (or ΔD_{it}) for various gate and drain biases and different channel lengths under pinch-off. This is shown in Figure 5 for calculated lifetimes according to Eq.(2) and using measured substrate and source currents.

In Figure 6, we plot the degradation of inverse transconductance ($\Delta(W/g_m)$) *vs.* normalized stress time $t/\tau_{W/gm}$, with $\tau_{W/gm}$ defined as the time to reach a change of 5.10^{-3} m/A/V. The hot-carrier-induced transconductance change can be shown to be (approximately) inversely proportional to the number of interface states [3]. Therefore, $\tau_{W/gm}$ and τ_{Icp} have a simple

correlation and we are able to calculate $\Delta(W/g_m)$ using Eq.(2).

CONCLUSIONS

To our knowledge, our formulation allows for the first time accurate NMOSFET interface state prediction for pinch-off stress conditions. It is easily implemented in a reliability circuit simulator and allows hot-carrier induced parameter drift to be modeled based upon the physical damage mechanism. Since interface states degradation is the predominant effect in NMOSFETs, this mechanism generally suffices to predict degradation of MOSFET transistor parameters and of the resulting degraded I-V characteristics at standard operating conditions.

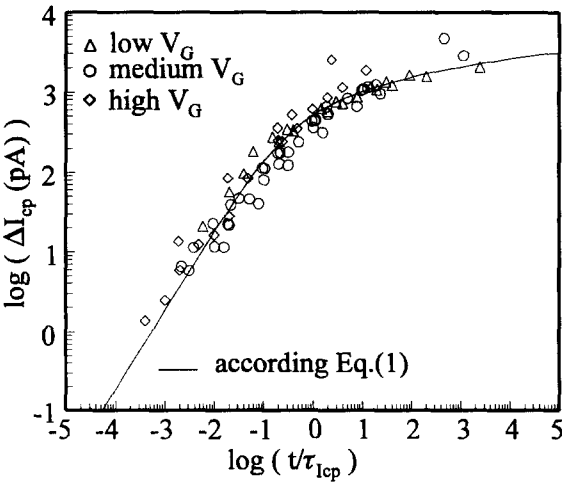

Figure 5. Predicted hot-carrier-induced increase in I_{cp} for conventional drain NMOSFETs (solid line). Lifetime τ_{Icp} was calculated using Eq.(2) using measured I_B, I_S, which may show spread from device to device, explaining the increased spread around the solid line.

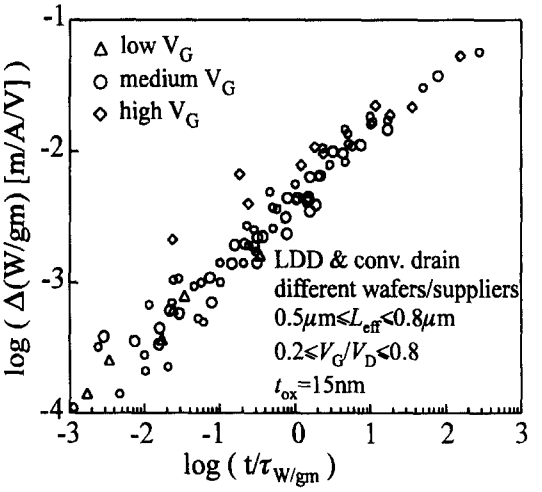

Figure 6. Inverse of NMOSFET transconductance degradation versus time normalized on lifetime $\tau_{W/gm}$, which is defined as the time at which $\Delta(W/g_m)= 5.10^{-3}$ m/A/V. Transconductance was measured at V_D=0.1V.

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