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Improvement of device characteristics by multiple step implants or introducing a C gettering layer

R.C.M. Wijburg[a,c], J.R. Liefting[a,b], J.S. Custer[b], H. Wallinga[a], and F.W. Saris[b]

[a]MESA Research Institute, University of Twente, P.O. box 217, 7500 AE Enschede, The Netherlands

[b]FOM Institute for Atomic and Molecular Physics, Kruislaan 407, 1098 SJ Amsterdam, The Netherlands

[c]Present address: Philips Semiconductors, MOS3 FB1.119, Gerstweg 2, 6534 AE Nijmegen, The Netherlands

Abstract

Ion implantation is used for realization of the collector in vertical bipolar transistors in a BiCMOS process. Secondary defects, remaining after annealing the implant damage, can give rise to an increased leakage current and to collector-emitter shorts. Two methods are proposed to avoid dislocation formation. First, by using multiple step implants, and second, by application of a carbon gettering layer. Experimental results show that these schemes can lower leakage currents, and moreover dramatically increase device yield. However, the carbon profile needs a further optimization with respect to the quality of the collector-substrate junction.

1. Introduction

Due to a reduced lateral diffusion of the dopants, high-energy ion implantation results in an increased packing density compared with processes using conventional buried layers [1]. The major problem with high-energy ion implantation is, however, the possible formation of dislocations after annealing [2]. These dislocations form if a critical amount of implant damage has been exceeded [3]. This issue applies particularly to the fabrication of collector regions, because the implanted dose must be sufficiently high to obtain a low collector resistance [1]. If the dislocations intersect a junction, an increased leakage current can result. When both the collector-base and emitter-base junctions are connected via a dislocation, collector-emitter shorts may arise by enhanced diffusion of the emitter dopant along the dislocation.

2. Dislocation Prevention

The quality of the transistors can be improved, if dislocation formation is avoided. We propose two methods to accomplish this. In the first method, the implant is performed in multiple steps, where each step generates a sub-critical amount of damage. Figure 1 shows that annealing a 1.1×10^{14} cm^{-2} 1 MeV phosphorus (P) implant gives rise to dislocations. If this implant, however, is performed in 4 steps of 2.8×10^{13}

cm^{-2} with after each step a 900 °C anneal for 15 min, no dislocations are observed.

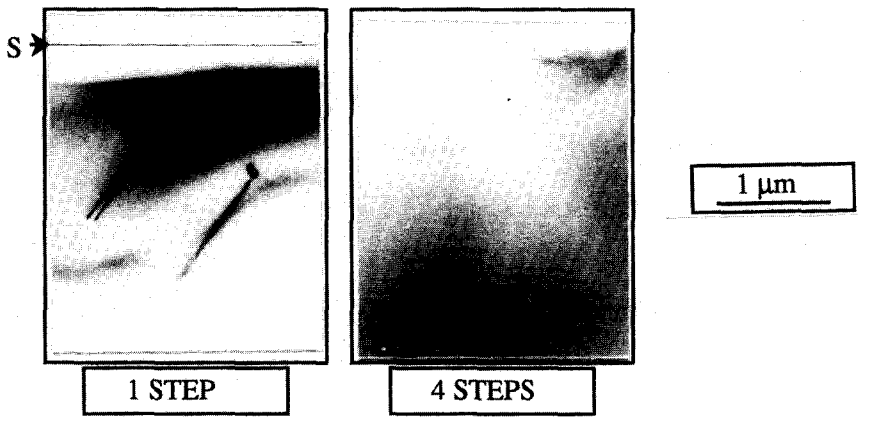

Figure 1: XTEM analysis of Si without and with multiple step implantation.

In the second method, carbon (C) is implanted in the damage region. It has been proposed that C acts as a sink for Si interstitials, thereby avoiding these insterstitials to agglomerate and form dislocations [4]. Figure 2 illustrates that annealing a $1x10^{14}$ cm^{-2} 725 keV boron (B) implant results in the formation of dislocations, whereas they can be avoided if $5x10^{14}$ cm^{-2} 800 keV C is co-implanted.

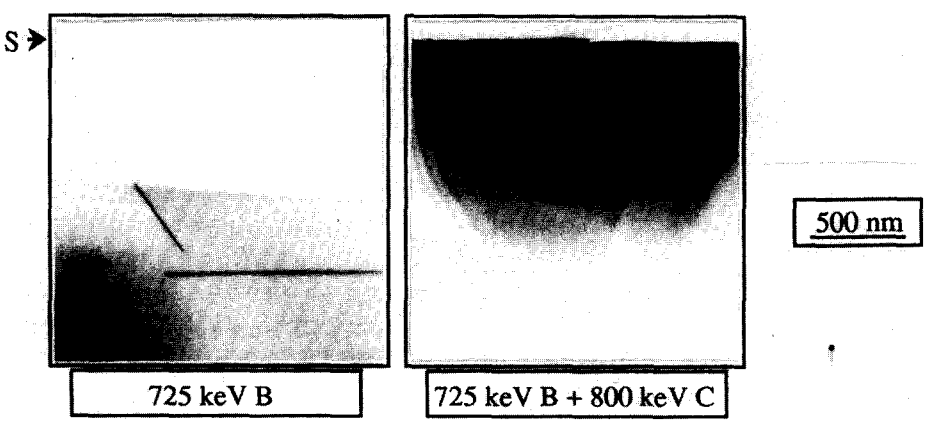

Figure 2: XTEM analysis of Si without and with co-implanted C.

Both methods are used to avoid dislocation formation for the $4x10^{13}$ P/cm^2 1.5 MeV collector implant in a BiCMOS process.

3. Sample Preparation

The collector and base of the bipolar devices in the BiCMOS process were formed after fabrication of the CMOS gates [1]. The collector of wafer 1 was implanted in two steps of $2x10^{13}$ cm^{-2} 1.5 MeV P, with each step followed by a 900 °C in N_2-ambient. Wafers 2 and 3, after a single $4x10^{13}$ cm^{-2} 1.5 MeV P implant, were partly co-implanted with 1.15 MeV C to doses of 2 and $5x10^{14}$ cm^{-2}, respectively. The projected range (R_p) of the C implant is about 0.2 μm deeper than the R_p of the P collector implant. These wafers were subsequently annealed at 900 °C for 15 min in N_2-ambient (see table 1). After annealing, a polysilicon emitter was made.

Table 1
Implants and treatments for collector region

	Wafer 1	Wafer 2	Wafer 3
Collector	$2x(2x10^{13}$ P/cm^2)	$4x10^{13}$ P/cm^2	$4x10^{13}$ P/cm^2
Carbon (partly)	---	$2x10^{14}$ C/cm^2	$5x10^{14}$ C/cm^2
Anneal	2x(900°C/15 min)	900°C/15 min	900°C/15 min

4. Experimental Results

Some of the Gummel plots of "standard" devices on wafers 2 and 3, i.e. without C implant, showed excessive collector current densities at low emitter-base voltages. This is attributed to the presence of collector-emitter shorts. The yield of these standard transistors as a function of the emitter area is plotted in figure 3. For cells with an emitter area of 10^4 μm^2, 65% of the emitters has a low resistive path to the collector, decreasing to 20% for devices with an area of 1200 μm^2. The larger the area, the higher the probability that at least one dislocation crosses both the emitter-base and collector-base junctions. As can be seen from figure 3, the yield of the devices with 2-step implanted collectors is nearly 100%. For the collectors co-implanted with C, no excess collector current behaviour is observed at all. Thus an enormous improvement is achieved compared to the results for the standard bipolar transistors.

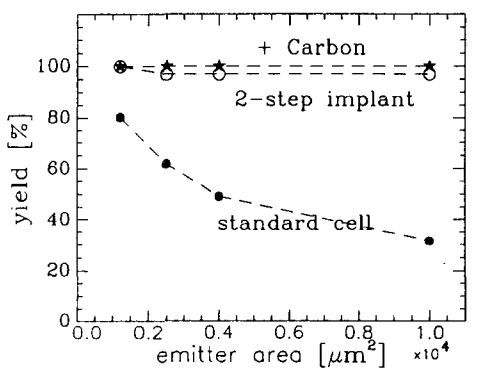

Figure 3: Yield of the bipolar transistors

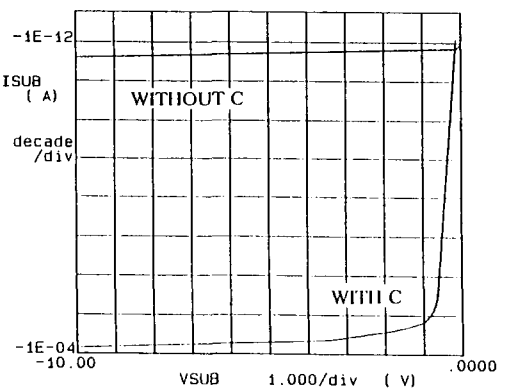

Figure 4: Typical collector-substrate leakage current behaviour (wafer 2)

The application of C as a gettering layer in the collector has also some disadvantages. It turned out that the sheet resistivity increased from 350 ohm/sq for the standard implanted collector to 540 and 630 ohm/sq for the 2 and $5x10^{14}$ C/cm^2 implanted structures, respectively. The leakage curent of the collector-substrate junction is, however, stronger influenced. Figure 4 shows typical leakage current characteristics of collector-substrate junctions on wafer 2. In the case of the higher C dose, the results are even worse.

C-related defects increase the leakage of the collector-substrate junction. On the other hand, the presence of carbon in the collector region lowers the leakage at the collector-base junction. Typical reverse characteristics, comparing C co-implanted devices with standard devices for wafer 3, are shown in figure 5. It is observed that the leakage currents are lower in the case of the higher C dose. The multiple step method also improves the leakage behaviour although not as well as the co-implanted C. This is presented in figure 6.

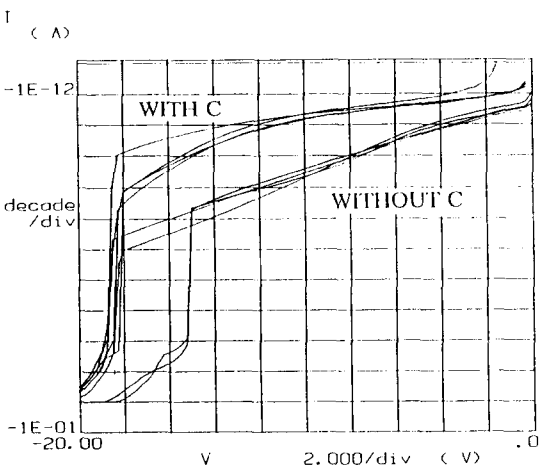

Figure 5: Collector-base leakage behaviour (wafer 3)

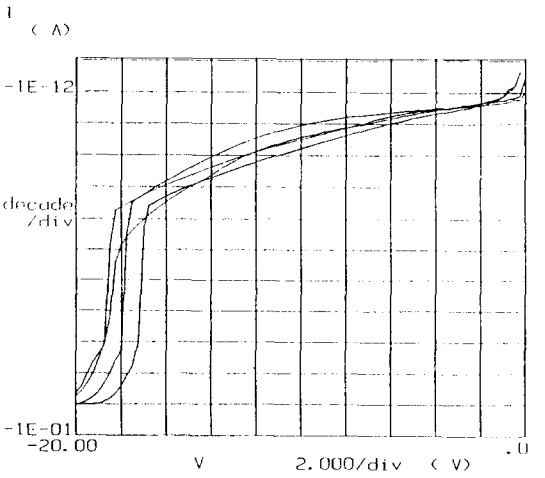

Figure 6: Collector-base leakage behaviour (wafer 1)

5. Conclusions

Two methods have been applied to suppress dislocation formation in bipolar transistors with ion implanted collector regions. In the first scheme, the collector was formed in two implant and anneal steps. In the second scheme, extra carbon was implanted in the collector region prior to annealing. Both methods drastically improve device yield. Besides, they lower the collector-base leakage current. However, the implanted C degraded the quality of the collector-substrate junction. This problem may be solved by adapting the energy and dose of the C implant.

6. References

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