

# Planar interdigitated electrolyte-conductivity sensors on an insulating substrate covered with Ta<sub>2</sub>O<sub>5</sub>

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## Abstract

Interdigitated electrolyte-conductivity sensors with an added top layer of insulating Ta<sub>2</sub>O<sub>5</sub> have been realized. The electrode-substrate structure under the Ta<sub>2</sub>O<sub>5</sub> film has been planarized in order to obtain a totally flat top surface. In addition, the electrodes have been applied on a totally insulating substrate, thus reducing the parasitic sensor capacitance by a factor of ten. © 1997 Elsevier Science S.A.

*Keywords:* Electrolyte-conductivity sensors; electrode-substrate structure; Ta<sub>2</sub>O<sub>5</sub>

## 1. Introduction

The measurement of electrolyte conductivity (EC) is common practice in analytical chemistry as well as in process industry. Good maintenance and non-continuous use of an EC sensor in a laboratory environment may prolong its useful life, whereas fouling of the sensor during continuous use in a process-line can shorten its life time considerably. EC determination in small sample volumes and in some in-line processes requires small dimensions of the sensor, which makes the effect of the non-ideal electrode-solution interfacial impedance increasingly problematic [1].

The problem of fouling as well as the effect of the electrode impedance play a less dominant role in the sensor behaviour, when the metal electrodes of the sensor are provided with a thin Ta<sub>2</sub>O<sub>5</sub> insulating film [2]. Fouling of this smooth, mechanically hard and chemically resistant surface is far less probable than fouling of a conventional rough, platinized electrode surface and, in addition, mechanical and chemical cleaning is facilitated. Moreover, the specific nature of the Ta<sub>2</sub>O<sub>5</sub> solution interface provides the electrode with a stable and relatively low oxide solution impedance, allowing sensor miniaturization. The desirability of

miniaturization as well as a monolithic sensor structure led to the interdigitated electrode structure as shown in Fig. 1(a) and (b) [3].

The cross-sectional view of the original design (Fig. 1(b)) shows that the Pt electrodes are applied on top of the SiO<sub>2</sub> layer on the Si substrate over which the insulating Ta<sub>2</sub>O<sub>5</sub> film is applied. This fabrication process has two consequences: first, the minimal thickness of the Ta<sub>2</sub>O<sub>5</sub> film is related to the thickness of the Pt electrodes in order to prevent cracks due to a bad step coverage at the Pt–SiO<sub>2</sub> step, and secondly, the Ta<sub>2</sub>O<sub>5</sub> top layer contains steps, comparable to that of the Pt electrodes. These consequences are disadvantageous: the resulting relatively thick Ta<sub>2</sub>O<sub>5</sub> film causes a sub-

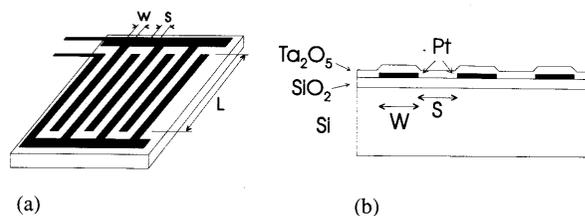


Fig. 1. (a) Impression of an interdigitated electrode pair showing the electrode width  $W$ , their length  $L$  and the interelectrode spacing  $S$ . (b) Cross-section of the previous device: an Si substrate with 1.3  $\mu m$  SiO<sub>2</sub> on top of which the 20 nm Ti + 75 nm thick Pt electrodes are evaporated. The total device is covered with a 120 nm thick insulating Ta<sub>2</sub>O<sub>5</sub> film [3].

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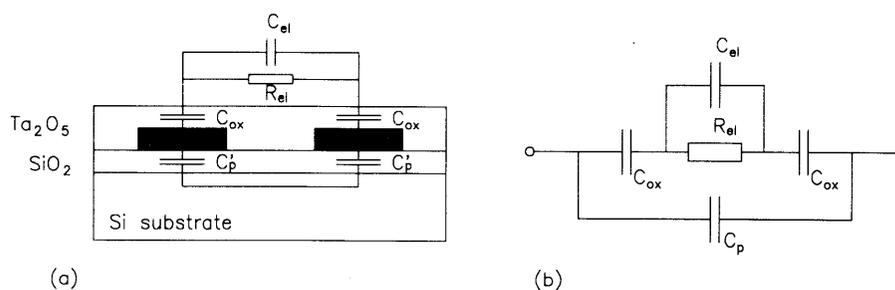


Fig. 2. (a) Cross section of the sensor with measurand  $R_{ei}$  and relevant parasitic components. (b) Equivalent circuit of the conductivity sensor. Note:  $C'_p = 2C_p$ .

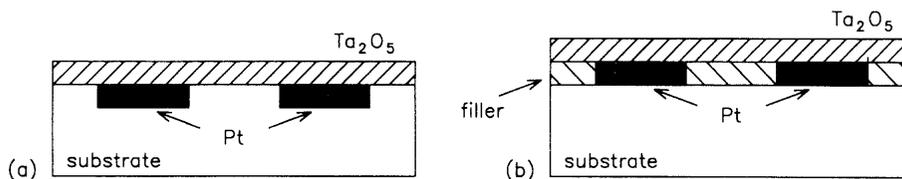


Fig. 3. Two methods to planarize the conductivity sensor: (a) by shallow etching in the substrate and (b) by deposition of filler material between the Pt electrodes.

optimal capacitive coupling to the solution and any subsequent modification of the top layer with an additional thin membrane (for biosensor applications) is difficult due to the steps in the Ta<sub>2</sub>O<sub>5</sub> surface.

An additional disadvantage of the former design is the parasitic capacitive coupling between the Pt electrodes and the conducting Si substrate via the 1.3  $\mu\text{m}$  thick SiO<sub>2</sub> film. The resulting parasitic capacitance, being parallel to the sensor impedance, causes a loss in sensitivity.

In this paper we propose a new method of sensor fabrication. In this method, the insulating substrate layer and the Pt electrodes form one planar surface on which a layer of Ta<sub>2</sub>O<sub>5</sub> is applied, which can be very thin as no steps have to be covered. Of course, the layer itself is now also without steps. Additionally, in the proposed method, the sensor structure is fabricated on a totally insulating substrate, thus greatly reducing the parasitic capacitance via the conducting substrate of the previous design.

The effect of the two proposed changes in the sensor fabrication can best be illustrated by an equivalent circuit of the original sensor, shown in Fig. 2(a) and (b). In Fig. 2, the double layer impedance is not included, on one hand because of the presence of  $C_{ox}$ , on the other hand because of the specific nature of the Ta<sub>2</sub>O<sub>5</sub> solution interface [2,3]. The effect of other remaining parasitic components is neglected. The introduction of an insulating substrate will greatly reduce the parasitic capacitor  $C_p$  and the use of a very thin Ta<sub>2</sub>O<sub>5</sub> layer on a flat sensor structure will noticeably increase the value of capacitor  $C_{ox}$ . Both proposed

modifications result in a more accurate and easy detection of the electrolyte resistance  $R_{ei}$ , which is the variable of interest.

The fabrication of the sensor will be treated and the effect of both the planarization and the absence of a conducting substrate will be shown.

## 2. Experimental

### 2.1. Device preparation

Several options, available for the choice of a non-conducting substrate have been evaluated:

#### 2.1.1. Si wafer with a very thick layer of SiO<sub>2</sub>

Because of the quadratic increase in oxidation time with the obtained thickness of the oxide, only a layer of maximally 3  $\mu\text{m}$  is realistic. This would reduce the capacitance  $C_p$  of Fig. 2 only marginally and, therefore, this option was discarded.

#### 2.1.2. Alumina wafers

It appeared that circular 3 in alumina wafers are not readily available. Moreover, the surface structure of alumina is rough, making this material unsuitable for the proposed planarized sensor.

#### 2.1.3. Quartz wafers

Quartz wafers are rather expensive and do not offer any particular advantage over glass for the application as substrate material, as pointed out in the next option.

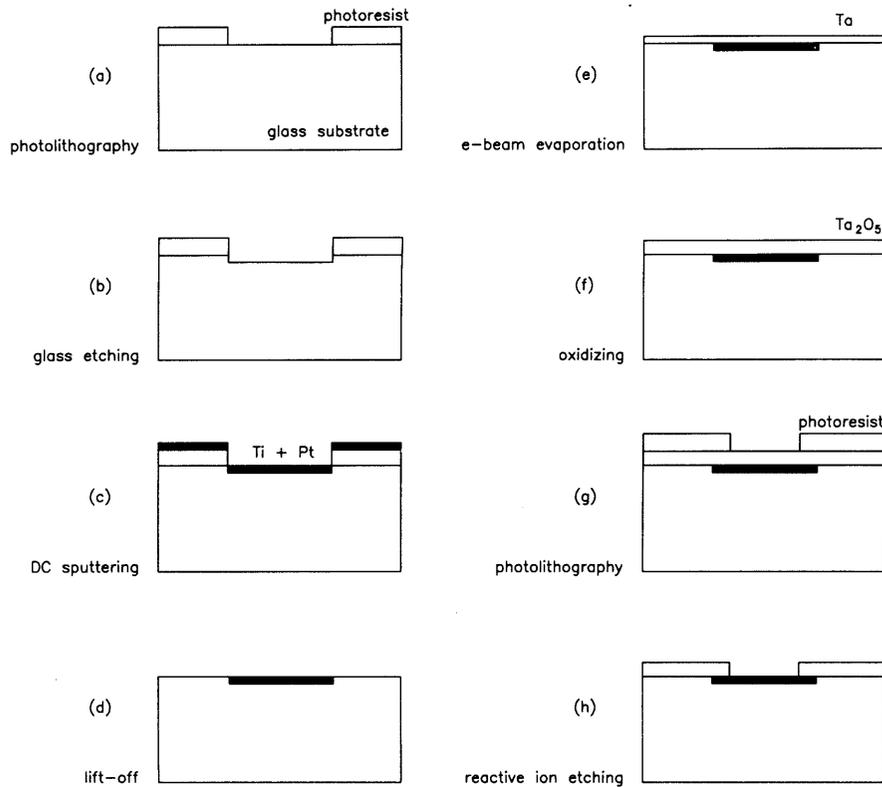


Fig. 4. (a–h) Process scheme of the planar EC sensor. (f) depicts the final sensor structure itself, (g) and (h) show the subsequent steps necessary for the contact holes. The process conditions are given in Table 1.

#### 2.1.4. Glass wafers

We decided to use glass wafers, which are readily available for anodic bonding purposes. These glass wafers, type Hoya SD2, have a very smooth top surface. The specific resistivity is  $4 \times 10^{16} \Omega \text{ cm}^{-1}$  and the dielectric constant is 6, both values at  $20^\circ\text{C}$ . Cheaper glass wafers are also available, but the many enclosed impurities might contaminate both the sensor and the process equipment during the high processing temperature of  $\text{Ta}_2\text{O}_5$  formation (about  $500^\circ\text{C}$ ).

Various technologies for planarization are already developed for integrated circuit processing. However, in those applications the preservation of electrical properties is the main issue, resulting in rather complicated processes [4]. For this reason, we developed our own technology to obtain a planar substrate Pt electrode top layer.

Principally, a planarized sensor can be obtained during processing in two different methods, depicted in Fig. 3(a) and (b). The electrodes can be applied on a flat substrate and the space between the electrodes can be filled with an insulating material to get a flat structure on top of which the  $\text{Ta}_2\text{O}_5$  film can be applied, as shown in Fig. 3(a). Another option is the etching of shallow channels in the substrate in which the elec-

trodes are deposited. Subsequently, the  $\text{Ta}_2\text{O}_5$  film can be applied on the flat structure, as shown in Fig. 3(b).

In this paper, a process based on the latter planarization method (Fig. 3(b)) is implemented. The proposed fabrication process is based on the previous one [3] and does not require new, complicated process steps. The new process is self-aligning, in that possible alignment problems of photo-masks on already etched structures do not occur. The consecutive steps of this process are schematically shown in Fig. 4(a–h).

Using the process depicted in Fig. 4 and described in more detail in Table 1, ten different designs of the EC sensor are produced on one wafer. The number of electrode fingers ranges from  $N=8-100$ , the finger width  $W=10-170 \mu\text{m}$ , their length  $L=500-1600 \mu\text{m}$  and the spacing between the fingers  $S=10-170 \mu\text{m}$ . Thus we obtained EC sensors with cell constants ranging from  $0.14-4.44 \text{ cm}^{-1}$  [3]. A number of these sensors were sawn from the wafer and the  $3 \times 4 \text{ mm}^2$  chips were glued on an  $8 \times 100 \text{ mm}^2$  printed circuit board (PCB) carrier and the Pt electrodes were connected to the copper strips on the PCB with standard wire bonding. The copper strips, the bonding wires and the edges of the chip were covered with epoxy for insulation and protection.

Table 1  
Details of the process steps as shown in Fig. 4

Step number	What?	How?
Fig. 4(a)	Photolithography	
Fig. 4(b)	Glass etching	HF:H <sub>2</sub> O = 1:50; 1 min @ 20°C; channel depth ≈ 90 nm
Fig. 4(c)	d.c. sputtering	Ti: 2 min and 40 s @ 200 W; layer ≈ 18 nm Pt: 3 min and 15 s @ 200 W; layer ≈ 75 nm
Fig. 4(d)	Lift-off	5 min in Aceton, then 30 s ultrasonic in Aceton
Fig. 4(e)	e-Beam evaporation	Ta: 32 s, 8 kV @ 5Å s <sup>-1</sup> ; layer ≈ 16 nm
Fig. 4(f)	Oxidizing	Ta: 3 h @ 500°C in O <sub>2</sub> ; layer ≈ 38 nm Ta <sub>2</sub> O <sub>5</sub>
Fig. 4(g)	Photolithography	
Fig. 4(h)	Reactive ion etching	Through Ta <sub>2</sub> O <sub>5</sub> ; 1 min, 50 mTorr @ 50 W; 30 sccm SF <sub>6</sub> and 5 sccm O <sub>2</sub>

## 2.2. Measurement set-up

The measurements in this paper are focused on the novel steps in the sensor preparation, i.e. the planarization and the use of an insulating substrate. The effect of the planarization was analyzed with a Sloan Dektak 3030 stylus surface profiler. Electrical characterization to determine the reduction of the parasitic capacitance with respect to the original design of Fig. 1 was performed with an HP 4194A impedance/gain-phase analyzer.

## 3. Results and discussion

The electrical characterization is restricted to measurements in air. The results of the measurements are given in Table 2 and suffice to show the effect of the introduction of an insulating substrate.

As expected in air, any resistive part in the measured results is absent and the sensor + probe leads behave like a pure capacitor. The probe leads themselves introduce a substantial part of the measured capacitance as can be seen from the results of Table 2. The capacitances of the leads can be cancelled out in practice by active shielding techniques. What is left then, as shown

Table 2  
Results of the electrical characterization in air of a Si- and glass-based EC sensor

	Probe leads (measured, pF)	Probe+sensor (measured, pF)	Sensor only (calculated, pF)
Si substrate	4.6	17.5	12.9
Glass substrate	4.6	5.8	1.2

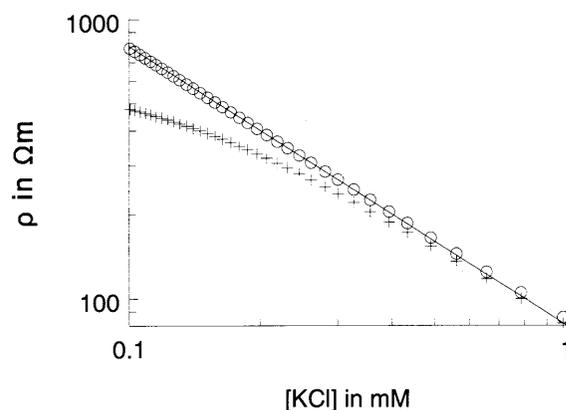


Fig. 5. Simulation results showing the relation between [KCl] and the corresponding specific resistivity ( $\rho$ ). Continuous line: theoretical relation; + markers:  $C_p = 12.9$  pF; O markers:  $C_p = 1.2$  pF. Other component values:  $C_{ox} = 600$  pF,  $C_{el} = 0.1$  pF. Measurement frequency: 200 kHz [3].

in the last column of Table 2, is the capacitance of the sensor only, which is in the case of the glass-based sensor a factor of 10 smaller than that of the Si-based sensor. This improvement can be translated either into a wider measurement range at equal accuracy or in a better accuracy at equal measurement range. This effect can be illustrated using the equivalent circuit of the sensor, shown in the introduction of this paper, Fig. 2(b). The relation between the KCl concentration and its corresponding specific resistivity is well known and is shown in Fig. 5 as a continuous line. Subsequently, measurements in KCl were simulated, using the circuit of Fig. 2(b) and Maple V (Waterloo Maple Software) to determine the specific resistivity,  $\rho$ , at a certain KCl concentration from the calculated sensor impedance, including its parasitic components. Using realistic component values found by measurements, shown in Table 2 and in the caption of Fig. 5; simulation results are shown in Fig. 5 both for the Si-substrate based sensor (markers: +) and for the glass-substrate based sensors (markers: O).

This figure clearly shows that the glass-substrate based sensor can successfully be used at low concentrations, without the need for any correction on the measured data and without loss in sensitivity.

The results of measurements showing the effect of the planarization are depicted in Fig. 6(a) and (b).

In Fig. 6(a), the result of a surface scan over the unplanar sensor top layer is shown. Clearly, the height

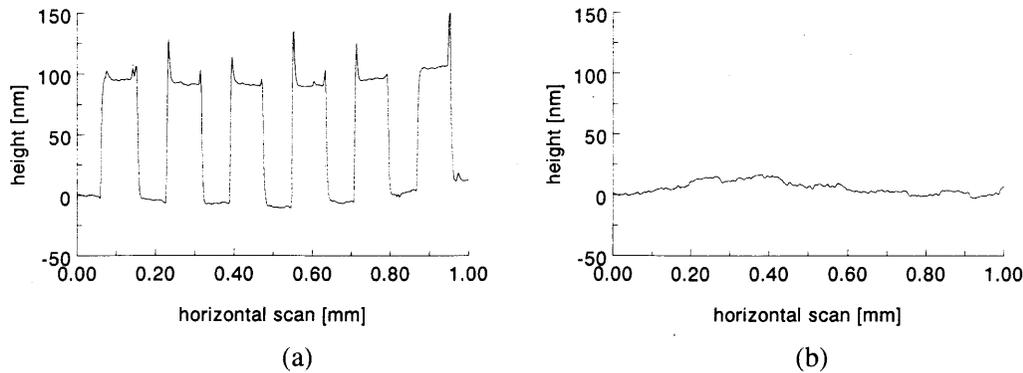


Fig. 6. Surface scan over an interdigitated EC sensor fabricated (a) according to the previous process (Fig. 1(b)), and (b) according to the new planar process of Fig. 4.

of the ridges in the  $Ta_2O_5$  top layer reflects the height of the Ti + Pt layer of 95 nm on top of the  $SiO_2$  substrate layer (see Fig. 1(b)). In Fig. 6(b), almost unnoticeable ridges of only a few nm remain, indicating the successful result of the new planar process of fabrication shown in Fig. 4. Subsequent measurements showing the benefits of this planar top layer, a better capacitive coupling to the solution via a thinner  $Ta_2O_5$  film and the feasibility to modify the EC sensor with (selective) membranes, are in progress.

#### 4. Conclusions

Interdigitated electrolyte-conductivity sensors have been realized with an added  $Ta_2O_5$  top layer, making fouling less likely and cleaning easy.

By a planar process of fabrication, the  $Ta_2O_5$  top layer of the EC sensor is totally flat within a few nanometers. Realization of the sensor on a insulating glass substrate has reduced the parasitic sensor capacitance by a factor of ten, from 12 down to 1.2 pF. The beneficial effect of the reduction of this parasite on the sensor performance has been shown by simulations.

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#### Biographies

*Wouter Olthuis* was born in Apeldoorn, the Netherlands, on October 23, 1960. He received the MS degree in electrical engineering from the University of Twente, Enschede, the Netherlands in 1986, and a PhD degree from the Biomedical Engineering Division of the Faculty of Electrical Engineering, University of Twente, in 1990. The subject of his dissertation was the use of Iridium oxide in ISFET-based coulometric sensor-actuator devices. Currently he is working as an Assistant Professor in the Biosensor Technology Group, part of the MESA Research Institute, of the University of Twente.

*Ad Sprenkels* received his MS and PhD degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1983 and 1988, respectively. During his PhD research his work was focused on silicon acoustic sensors with the necessary dedicated electronics. From 1988 until 1990 he has been working as a sensor engineer with 3T. In 1990 he joined the R&D department of Microtel and was involved in the development of various hearing aid transducers. Since 1994 he has worked as a consultant on micro system technology and analog electronics.

*Johan Bomer* was born in Eibergen, The Netherlands, on September 6, 1958. He received the BS degree in applied physics from the Hoger Technische School, Enschede, The Netherlands, in 1981. From 1983 until 1986 he worked as technologist in the Semiconductor Physics Group of the University of Groningen. Since 1986 he has worked as a technologist in the Biosensor Technology Group, part of the MESA Research Institute, of the University of Twente.

*Piet Bergveld* was born in Oosterwolde, The Netherlands, on January 26, 1940. He received the MS degree

in electrical engineering from the University of Eindhoven, the Netherlands, in 1965 and a PhD degree from the University of Twente, the Netherlands, in 1973. The subject of his dissertation was the development of ISFETs and related devices, the actual invention of the ISFET, since also investigated by many international research groups of Universities, as well as industry. Since 1965 he has been a member of the Biomedical Engineering Division of the Faculty of Electrical Engi-

neering (University of Twente) and was in 1984 appointed as Full Professor in Biosensor Technology. He is one of the project leaders in the MESA Research Institute. His research subjects still concern the further development of ISFETs and biosensors based on ISFET technology as well as physical sensors for biomedical and environmental applications, resulting up to now in more than 250 papers.