A Radiation Hard Bandgap Reference Circuit in a Standard 0.13 μm CMOS Technology

Vladimir Gromov, Anne Johan Annema, Ruud Kluit, Jan Lammert Visschers, *Member, IEEE*, and P. Timmer

***Abstract*—With ongoing CMOS evolution, the gate-oxide thickness steadily decreases, resulting in an increased radiation tolerance of MOS transistors. Combined with special layout techniques, this yields circuits with a high inherent robustness against X-rays and other ionizing radiation. In bandgap voltage references, the dominant radiation-susceptibility is then no longer associated with the MOS transistors, but is dominated by the diodes. This paper gives an analysis of radiation effects in both MOS devices and diodes and presents a solution to realize a radiation-hard voltage reference circuit in a standard CMOS technology.**

A demonstrator circuit was implemented in a standard 0.13 μm CMOS technology. Measurements show correct operation with supply voltages in the range from 1.4 V down to 0.85 V, a reference voltage of 405 mV $\pm$ 7.5 mV ($\sigma = 6$ mV chip-to-chip statistical spread), and a reference voltage shift of only $\pm$1.5 mV (around 0.8%) under irradiation up to 44 Mrad (Si).

***Index Terms*—Bandgap voltage reference, CMOS, DTMOS, low voltage, radiation.**

I. Introduction

REFERENCE voltage generating circuits with low sensitivity to temperature variation and power supply variations are commonly used in analogue blocks such as voltage regulators, A/D and D/A converters. In some applications like circuits for the aerospace industry and for high-energy physics experiments, there is an additional requirement to deliver a stable voltage even when operating in ionizing radiation environments [1].

Historically, rad-hard ASIC's for military and space applications were fabricated in silicon-on-insulator (SOI) or silicon-on sapphire (SOS) technologies [2], [3]. Compared to mainstream silicon technologies, SOI reduces the radiation sensitive volume by isolating the entire device from the bulk substrate with the help of the buried oxide layer. This makes SOI highly resistant to single event upsets (SEU), furthermore because SOI has no wells in the substrate, an irradiation triggered single event latch-up (SEL) cannot occur. However, commercial SOI is still sensitive to the total ionizing dose (TID). This effect originates in the fact that charge induced by gamma rays or X-rays gets trapped in the buried oxide. The accumulated charge causes a major performance degradation of the analogue blocks through the mechanism of a shift of the threshold voltage in MOS structures [4], [5]. Therefore SOI requires special technological hardening steps to achieve a sufficient level of robustness to TID [6].

Recently, however, ASIC's fabricated in standard deep-submicron CMOS technologies have demonstrated robustness to SEL and TID, when special design topologies like enclosed (edgeless) transistor geometry and guard rings are used [4], [7], [8]. Without using a buried oxide, deep-submicron CMOS technologies have inherently a high tolerance to TID due to the reduced thickness of the gate oxide ($t_{ox} = 2.2$ nm). This phenomenon is caused by quantum tunneling of electrons into the gate oxide, which allows for recombination of the radiation-induced holes, before converting of the holes into interface states [9], [10].

The objective of this work is to design a high quality voltage reference circuit in a standard commercial 0.13 μm CMOS technology capable of operating in harsh radiation environments.

This paper is organized as follows. Section II presents a review of TID effect in MOS devices, the impact of scaling of CMOS technology on its susceptibility to ionizing radiation and discusses some radiation-tolerant layout issues. Section III describes the evolution of the bandgap reference circuit towards a radiation hard solution. Fundamentals of the CMOS bandgap voltage reference are covered in Section IV. Sections V and Section VI discuss the proposed solution for a bandgap voltage reference circuit and the characterization of its core component (dynamic-threshold MOS transistor). Section VII presents the experimental results. The conclusions are summarized in Section VIII.

II. Total Ionizing Dose Effects in MOS Devices

An accumulated flux of high energetic charged particles and gammas leads to total ionizing dose (TID) effects in MOS devices, which manifest themselves mainly as shifts in the MOS flat-band voltage [11]. TID effects are caused by the creation of free electron-hole pairs in any oxide volume when radiation passes through. The number of such electron-hole pairs depends on the total ionization energy deposited inside the oxide, at several eV per e-h pair. Due to the presence of a high electric field in the gate oxide, charge carriers that escape direct recombination remain separated. Another effect of the strong electric field is that the electrons in the oxide become highly mobile and are swept out of the thin oxide in a matter of picoseconds after the ionization. However, the low-mobility holes will migrate only slowly to the cathode, as depicted in Fig. 1 [12].

Manuscript received April 11, 2007; revised September 20, 2007. This work was supported in part by Dutch National Institute for Subatomic Physics (Nikhef) and the University Twente, Enschede, The Netherlands.

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Digital Object Identifier 10.1109/TNS.2007.910170

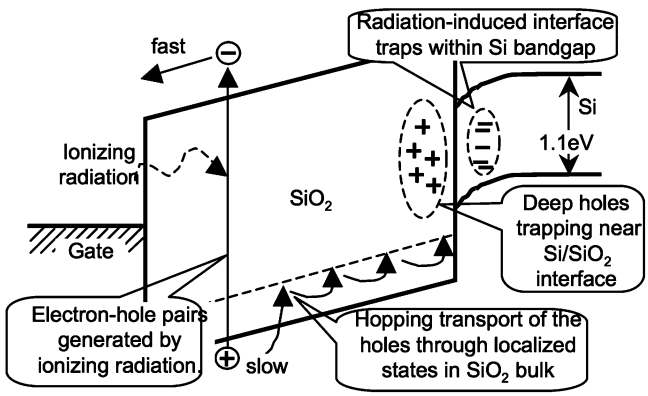

Fig. 1. Schematic representation of basic radiation effects in gate oxide of NMOS device.

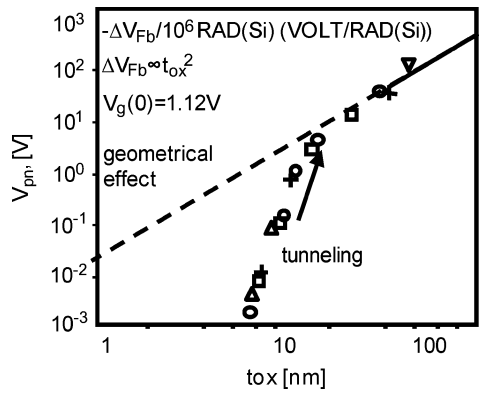

Fig. 2. Radiation-induced shift of the flat-band voltage for MOS capacitors due to oxide trapped charge as a function of the oxide thickness $(\mathrm{t_{ox}})$ [11].

A fraction of these holes may leave the dielectric but the other holes get trapped in pre-existing lattice defects near the $\mathrm{SiO_2-Si}$ interface. The presence of the trapped holes changes the electric field in the channel below the gate oxide and therefore causes a threshold voltage shift in a MOS structure. Part of this threshold shift is recovered after some time due to two processes. The first is the short-term (from 1 μs up to 1 s) transport of free holes outside the dielectric. The second is that some trapped holes create interface states within the silicon (Si) bandgap. These traps will recover by recombination, which is a long-term process (from 1 s to infinity) that occurs with a ln(time) dependence [12]. Note that this implies that the threshold of MOS structures drifts both during and after irradiation.

Scaling of a CMOS technology implies a reduction of the lateral dimensions of the circuit, while at the same time reducing the thickness of the gate oxide $(\mathrm{t_{ox}})$. It has been found [11] that radiation-induced shift of the threshold voltage in MOS devices scales approximately proportional to $\mathrm{t_{ox}^2}$ (see Fig. 2) for thick gate oxide devices $(\mathrm{t_{ox}} > 12\ \mathrm{nm})$. For thinner oxides $(\mathrm{t_{ox}} < 12\ \mathrm{nm})$ the threshold voltage shift deviates considerably from this power-law behavior (see Fig. 2), which is caused by quantum-tunneling of free electrons from the channel into the radiation-induced holes in the oxide before they can convert to interface trapped states [13].

For 0.13 μm CMOS technology, the gate oxide thickness is 3 nm or less [14]. Therefore the TID effects occurring in the gate oxide do not play a dominant role for the threshold shift in the MOS transistor. The dominant source for TID effects is then the presence of thick $(\mathrm{t_{ox}} > 12\ \mathrm{nm})$ isolation field oxide around MOS devices. In this field oxide a pair of parasitic channels can be formed due to TID effects if the MOS transistor is designed in the standard linear layout [15]–[17]. These parasitic side channels corrupt the characteristics of the whole device, especially for narrow transistors (small W/L). Since radiation produces only positive charges (free or trapped holes) in the body of the field oxide, the threshold voltage increases in p-channel devices, while the threshold voltage in n-channel devices decreases.

To eliminate the parasitic channels, the enclosed layout transistor (ELT) was introduced [5], [7]. In this geometry the gate completely surrounds the source of the transistor, avoiding any parasitic channels. The removal of the parasitic channels eliminates the threshold shift caused by ionizing radiation in field oxide. To reduce the risk of radiation triggered single-event latch-up, it is common practice to use low-ohmic guard rings around every p-well and n-well. The ELT with guard rings in deep submicron CMOS technologies proves to be an extremely radiation tolerant MOS device.

III. Radiation Tolerant Layout Approach for Bandgap Reference Circuits

The bandgap reference circuit [18], [19] is commonly used to implement a reference voltage generator. The operation of this type of circuit relies on the properties of the forward-biased p-n junction (diodes). However, with steady progress in downscaling of CMOS technologies, the use of bandgap reference circuits with conventional diodes in radiation hard environments has two distinct disadvantages. Firstly, the low supply voltage in modern CMOS technologies significantly complicates the bandgap reference circuit design when conventional diodes are used [20]–[22]; a suitable approach using conventional diodes was introduced by Banba [23]. Secondly, it has been found that bandgap references featuring conventional diodes are rather vulnerable to TID effect [24]. Detailed analysis of the behavior of conventional bandgap references in deep submicron CMOS technology indicates that radiation damage in diodes is the main cause of reference voltage shifts [25]. A short discussion of this is presented below.

In conventional bandgap reference circuits in CMOS, the diodes are usually implemented using a p-diffusion in (grounded) n-well (see Fig. 3). A shallow trench isolation field oxide layer surrounds the p-diffusion area. As discussed in Section II, irradiation-induced holes get trapped in the body of field oxide near the $\mathrm{SiO_2-Si}$ interface [26]. This phenomenon can cause radiation-induced change of the I-V characteristic of the diode. For radiation doses up to 79 Mrad, about 4% shift in the reference voltages, due to this effect, has been found [25].

The main cause of the voltage shifts in (well designed) CMOS bandgap references in radiation hard environments is the charging of the field oxide that surrounds the p-diffusion area. A possible solution of this problem could be replacing the (thick and radiation-intolerant) field oxide next to the p-diffusion by thin radiation-tolerant (see Section II) gate-oxide. In this way

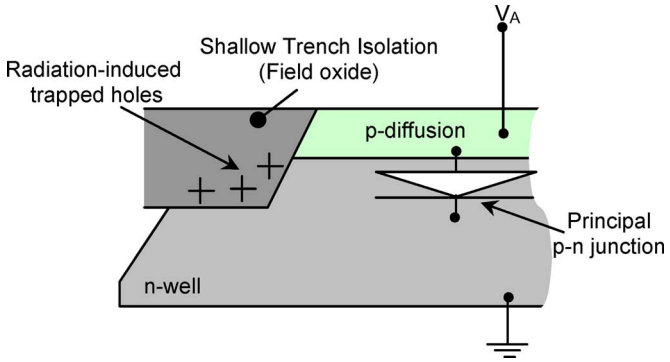

Fig. 3. Conventional diode in the 0.13 μm CMOS: p-diffusion in a grounded n-well.

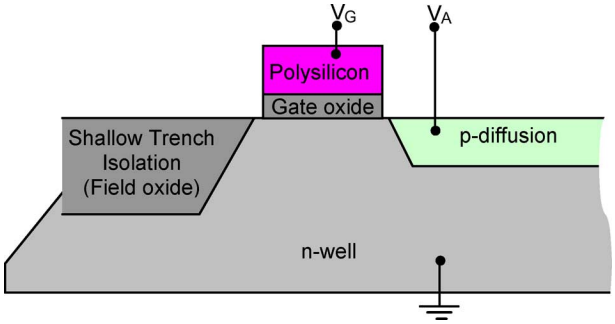

Fig. 4. Gated diode.

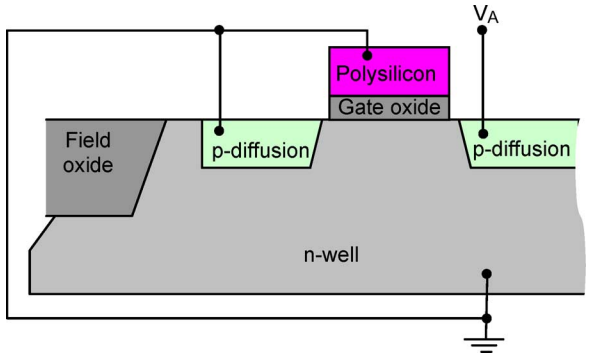

Fig. 5. Dynamic-threshold MOS transistor (DTMOST).

two structures can be obtained: the gated diode shown in Fig. 4 and the conventional PMOS transistor. The gated diode has been proposed to be used for the assessment of radiation damage [27]. However, this device is not allowed to be implemented in our CMOS technology because of design-rule limitations.

The second way to avoid field oxide adjacent to a pn-junction is using a MOS transistor layout in which the source-well junction is used as diode. In order to get conventional diode-like behavior, the effect of the gate must be either minimized or well defined. One possibility is tying the gate to a high voltage, which is not a simple solution in low voltage CMOS technologies. The other possibility is tying the gate to the p-diffusion (drain) to obtain a constant effect of the gate on the diode's behavior. The corresponding device is shown in Fig. 5. The so-obtained structure is called dynamic-threshold MOS transistor (DTMOST) [28], [31]; in Section IV the electrical properties of the DTMOST are discussed in detail. In short, this device can be operated as a diode with a low effective bandgap. In our design we used a P-channel DTMOS-diode that can be realized in any twin well (p-bulk) CMOS process.

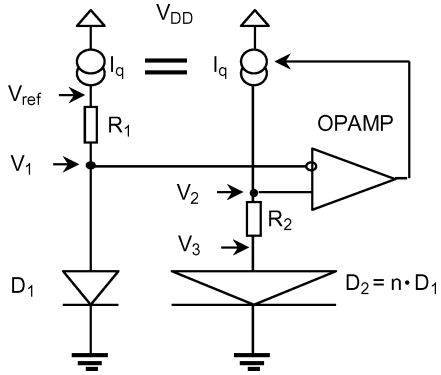

Fig. 6. Typical CMOS bandgap voltage reference circuit.

The internal p-diffusion area (source) of the DTMOST can be surrounded by gate oxide to form enclosed layout geometry. In this way, the device is inherently radiation hard due to the absence of any thick oxide near the pn-junction.

IV. Fundamentals of the CMOS Bandgap Voltage Reference

A. Typical CMOS Bandgap Voltage Summing Reference

A typical CMOS bandgap reference circuit is shown in Fig. 6. The reference voltage depends heavily on the characteristics of the diodes. The current-to-voltage characteristic of a p-n junction is:

$$i_D = I_0 \cdot \left(e^{\frac{q \cdot v_{PN}}{kT}} - 1\right) \tag{1}$$

In (1), I_0 is the leakage current, q is the electron charge, k is Boltzmann's constant and T is the absolute temperature of the junction. For an abrupt junction, I_0 is [29]:

$$I_0 = const \cdot A \cdot T^{3+\gamma/2} \cdot e^{\frac{-E_g}{kT}} \tag{2}$$

where A is the area of the junction, E_g is material bandgap, and γ is a constant which is related to the temperature dependence of the mobility and the diffusion coefficients of the minority carriers. The voltage-to-current relation for a forward biased diode is then:

$$V_{PN} = V_g(T) + \frac{kT}{q} \ln\left(\frac{I}{const \cdot A \cdot T^{3+\gamma/2}}\right) \tag{3}$$

In this relation, $V_g(T) = E_g(T)/q$ is the bandgap voltage. It is important to notice that the voltage across a p-n junction is about Conversely Proportional to Absolute Temperature (CTAT) (see Fig. 7). For $T \to 0$ the value of V_{PN} approaches $\mathrm{V_g(T=0)}$ regardless of the current; in silicon $\mathrm{V_g(T=0)}$ is 1.12 V. The operating current I_q in the circuit is determined by the following condition:

$$V_1(I_q) = V_2(I_q) \tag{4}$$

and hence

$$I_q = \frac{V_1(I_q) - V_3(I_q)}{R_2} \tag{5}$$

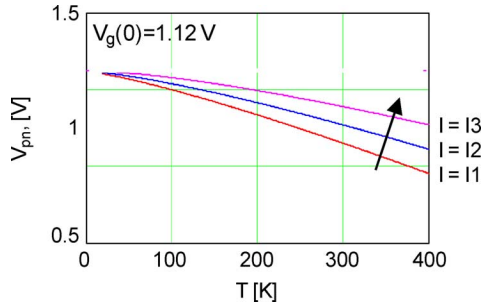

Fig. 7. Voltage across a p-n junction as a function of temperature.

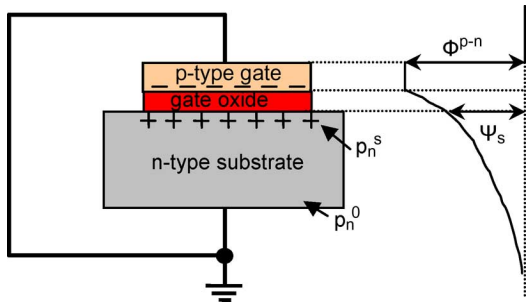

Fig. 8. MOS structure with the gate tied to the n-type substrate.

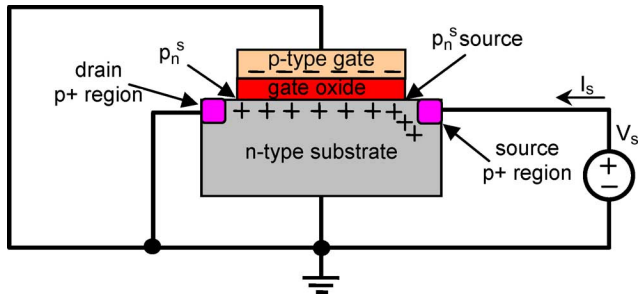

Fig. 9. DTMOST diode: MOS-transistor with the gate tied to the n-well and the drain.

where V_1 and V_3 are the voltages across diodes D_1 and D_2. Assuming that the diodes D_1, D_2 differ only in size and taking into account (3):

$$I_q = \frac{kT}{q \cdot R_2} \ln(n) \tag{6}$$

where n is the ratio of the emitter areas of the diodes. Note that $I_q(T)$ is Proportional to Absolute Temperature (PTAT) [30]. The reference voltage is the sum of the CTAT voltage source $\mathrm{V}_1(\mathrm{T})$ and the PTAT voltage drop on resistor R_1:

$$V_{ref}(T) = V_1(T) + \frac{kT \cdot R_1}{q \cdot R_2} \ln(n) \tag{7}$$

Resistors R_1, R_2 determine the temperature slope of the PTAT which compensates for the CTAT shift. The typical CMOS bandgap voltage reference circuit (see Fig. 6) generates an output voltage close to 1.22 V, which is the bandgap voltage, extrapolated from the operation temperature to 0 K. In 0.13 μm CMOS technology the nominal power supply voltage is as low as 1.2 V, which is clearly insufficient for this type of bandgap reference circuit.

B. Radiation Hard CMOS Bandgap Voltage Reference With DTMOSTs

The aim of this work is to design radiation tolerant bandgap voltage reference circuits. As discussed in Section III, the dynamic-threshold MOS transistor [31] in ELT layout is inherently robust to radiation effects and has a diode-like current-voltage relation. Therefore we have chosen a DTMOST-based architecture for the design of the circuit.

Fig. 8 represents a MOS structure with the gate and the n-type substrate contacts connected together [28]. The built-in potential for the heavily doped p-type gate and the n-type substrate, $\Phi_{\mathrm{p-n}}$ is about -1 V when the substrate doping concentration N_D is about 10^{17} cm^{-3} [29]. This built-in voltage partly drops in the substrate, making a potential Ψ_{s} on its surface. In the depletion and weak inversion region Ψ_{s} is a fraction of $\Phi_{\mathrm{p-n}}$ which follows:

$$\Psi_s = \frac{\Phi^{pn}}{n_0} \tag{8}$$

where $n_0 = 1.2 \ldots 1.6$ (process dependent), and therefore

$$\Psi_s \approx -0.8 \ldots -0.6 \tag{9}$$

Due to the built-in potential the surface concentration of holes $\mathrm{p}_{\mathrm{n}}^{\mathrm{s}}$ exceeds the equilibrium concentration of holes $\mathrm{p}_{\mathrm{n}}^{\mathrm{o}}$ in the bulk of the substrate as follows:

$$p_n^s = p_n^0 \cdot e^{\frac{q \cdot |\Psi_s|}{kT}} \tag{10}$$

since

$$p_n^0 = \frac{n_i^2}{N_D} \tag{11}$$

$$n_i = const_1 \cdot T^{3/2+\gamma/4} \cdot e^{\frac{-E_g}{2kT}} \tag{12}$$

where n_i is the intrinsic carrier concentration, N_D is the doping concentration in the substrate. Taking into account (10), (11) and (12), the surface concentration of holes is:

$$p_n^s = const_2 \cdot T^{3+\gamma/2} \cdot e^{\frac{-q \cdot (V_g - |\Psi_s|)}{kT}} \tag{13}$$

Expression (13) demonstrates that due to the effect of the built-in potential, the surface concentration of minority carrier's increases and the effective bandgap voltage is lowered:

$$V_g^{eff} = V_g(T) - |\Psi_s| \approx 0.3 \text{ V} \ldots 0.5 \text{ V} \tag{14}$$

The DTMOST diode is in fact a PMOS transistor with gate, drain and substrate contacts connected together (see Fig. 9). The hole concentration on the surface is uniform given by (13) except for the region close to source. An external applied voltage changes the concentration at the source terminal as follows:

$$p_n^s source = p_n^s \cdot e^{\frac{V_s}{\Phi_t}} \tag{15}$$

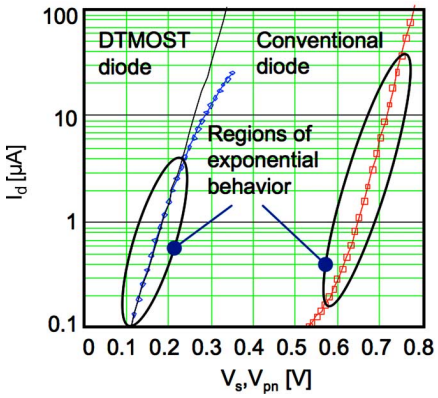

Fig. 10. Current-to-voltage characteristics for both DTMOST configuration and for the conventional diode configuration.

We restrict the analysis of the device's operation to the weak inversion region. In this region the source current $\mathrm{I_s}$ is caused by the diffusion of the inverse charge on the surface as follows [32]:

$$I_s = \frac{W}{L} \cdot \mu \cdot \frac{kT}{q} \cdot \left(\mathrm{Q'_{I,source}} - \mathrm{Q'_{I,drain}}\right) \tag{16}$$

Where W and L are the width and the length of the device, μ is the surface mobility of holes and $\mathrm{Q'_I}$ is the inversion charge per unit area, which is proportional to the surface concentration of holes:

$$Q'_I = Const_3 \cdot p_n^s. \tag{17}$$

Using (13)–(17) the source current becomes:

$$I_s = I_{so} \cdot \left(e^{\frac{V_s}{\Phi_t}} - 1\right), \tag{18}$$

where the saturation current $\mathrm{I_{so}}$ is:

$$I_{so} = Const_3 \cdot \frac{W}{L} \cdot T^{4+\gamma/2} \cdot e^{\frac{(-E_g - q)\cdot|\Psi_s|}{kT}}. \tag{19}$$

Comparing (18) and (19) with (1) and (2) it is apparent that a conventional p-n junction and the DTMOST diode (in the restricted region of weak inversion) demonstrate identical exponential current-to-voltage characteristics (see Fig. 10). However, the saturation current is much higher for the DTMOST diode due to the built-in potential factor $e^{(q\cdot|\Psi_s|)/kT}$

The exponential character of the current-to-voltage relation of the DTMOST diode in weak inversion (18) enables the construction of a PTAT voltage source using the approach described for typical CMOS bandgap voltage reference. Due to the effect of effective lowering the bandgap voltage (14), the reference voltage of the present circuit will be much lower than that for the typical CMOS bandgap voltage reference. It can be concluded that a bandgap reference circuit using DTMOST diodes, see Fig. 11, may be used to implement a low voltage and radiation tolerant voltage reference, in standard CMOS technology.

V. Characterization of the DTMOST

For modeling of DTMOST transistors with low to medium accuracy, ordinary MOS models such as BSIM3v3 or MOS11 are sufficient. However, if accurate modeling is needed, as is the case when using these devices as diodes in voltage references, a dedicated model is required [33]. For this work, characterization of the DTMOST was done in only the region of interest: at various temperatures in only the region where the I-V relation is exponential.

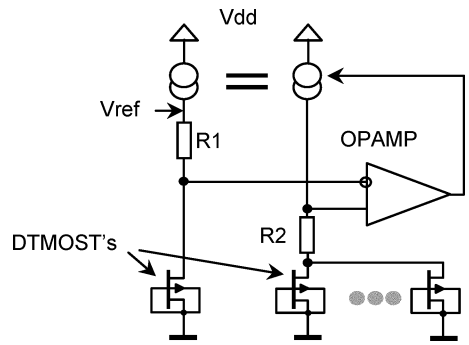

Fig. 11. Architecture of the bandgap voltage reference circuit with DTMOST-diodes.

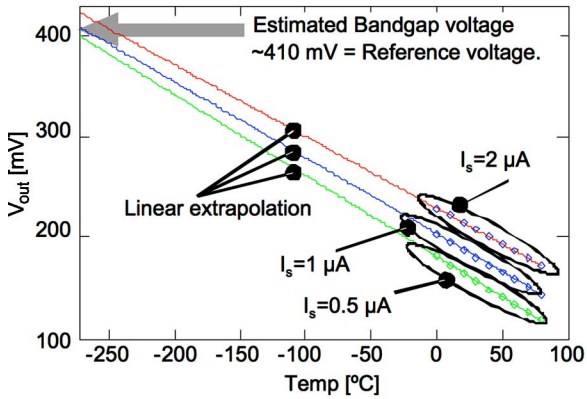

Fig. 12. Voltage across the DTMOST at various currents as a function of temperature.

The measurements confirm that the voltage across the DTMOST is conversely proportional to absolute temperature (see Fig. 12) when the device operates in the region of exponential behavior. By extrapolating the $\mathrm{V_s(T)}$ curves at various bias currents to $\mathrm{T} = 0\ \mathrm{K}$, the effective bandgap voltage is estimated to be 410 mV, with a temperature gradient (at constant current) of about $0.8\ \mathrm{mV/^{\circ}C}$.

VI. Bandgap Voltage Reference Circuit

The designed bandgap voltage reference circuit is a straight forward circuit, consisting of two DTMOST's, a pair of cascoded current sources and a two-stage operational amplifier. The circuit schematic is shown in Fig. 13; the layout is shown in Fig. 14.

All MOS devices of the circuit are designed in the gate enclosed geometry with guard rings to guarantee radiation tolerance. The die area of the reference circuit, without pads, is 0.065 $\mathrm{mm^2}$.

VII. Experimental Results

A. Temperature Dependence of the Reference Voltage

Measurements were done on 12 unselected samples. To be able to clearly identify the radiation-sensitive parts of the cir-

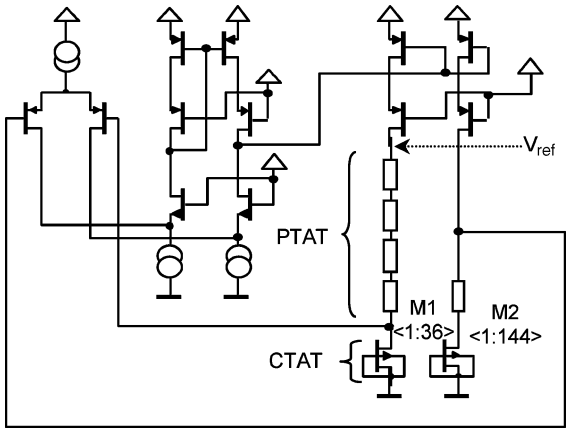

Fig. 13. Schematic of the radiation hard voltage reference circuit.

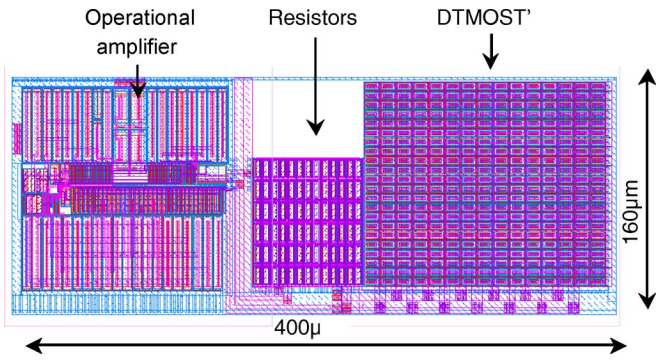

Fig. 14. Layout of the radiation hard voltage reference circuit.

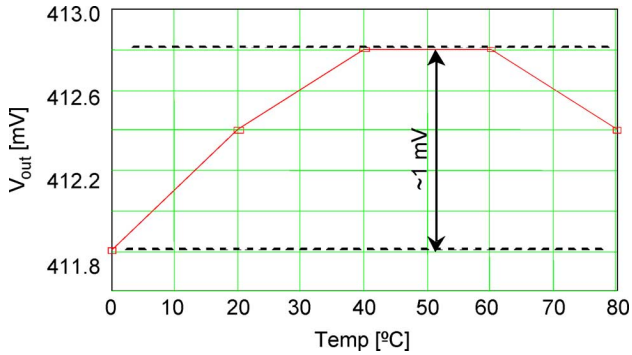

Fig. 15. Measured reference voltage as a function of temperature. Optimal temperature compensation.

cuit, the PTAT resistor (see Fig. 13) has been divided in sections, so that they can be bypassed externally. In this way the slope of the PTAT voltage has been trimmed to the slope of the CTAT voltage in order to get the minimum temperature coefficient of the reference voltage. Under this condition the reference voltage to temperature relation is a parabola with maximum deviation around 1 mV within the range from 0°C up to 80°C (see Fig. 15). Without trimming, the temperature coefficient of the reference voltage ranges from $-0.1\ \mathrm{mV/°C}$ to $+0.2\ \mathrm{mV/°C}$.

B. Fluctuation of the Reference Voltage Caused by X-Ray Irradiation

CERN's in-house X-ray (10 keV) facility [34] was used for the irradiation of the chips. The irradiation resulted in a

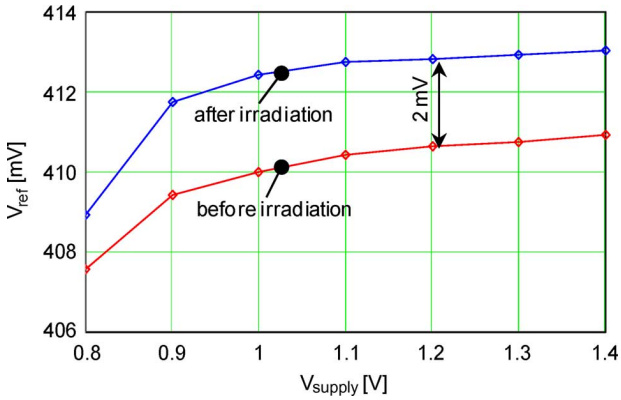

Fig. 16. Measured reference voltage as a function of power supply voltage before and after irradiation. Accumulated dose is 40 Mrad.

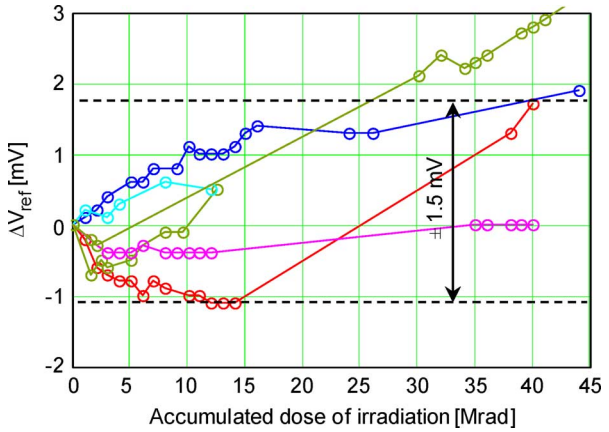

Fig. 17. Measured shift of the reference voltage during irradiation for 6 prototype chips. All MOS structures of this circuit are designed in the gate enclosed geometry with guard rings to guarantee radiation tolerance.

moderate shift of the reference voltage. For one (unselected) sample the reference voltage versus supply voltage dependency is shown before and after irradiation; irradiated with X-rays dose as high as 40 Mrad, the reference voltage shift amounts to only a few mV (see Fig. 16).

The change of the reference voltage as a function of the radiation dose is shown in Fig. 17; for clarity reasons the results of only 6 (unselected) samples are shown. The measurements show that the effect of the radiation is fluctuating heavily. However, in all cases, the reference voltage fluctuation range is less than 1% for doses up to 40 Mrad. This change is much lower than the typical 4% change at 79 Mrad for bandgap references using conventional diodes [25].

To clearly demonstrate the effectiveness of the radiation tolerant layout approach [5], [7], the same bandgap reference circuit was designed using the standard linear layout MOS transistors all over the design except for the DTMOST's structures. The DTMOST's were in the enclosed layout transistor geometry. Measurements on this circuit show a significantly worse radiation tolerance: the reference voltage fluctuation range is about 12 mV or 3% when being irradiated up to 44 Mrad.

C. Chip-to-Chip Spread of the Reference Voltage.

In some applications not only the stability of the reference voltage is important, but also its absolute value. The absolute

TABLE I
MEASURED SPECIFICATIONS

Power supply voltage	0.85 V $< V_{DD} <$ 1.4 V
Area	0.064 mm^2
Reference voltage	V_{ref} = 405 mV ±7.5 mV (chip-to-chip spread)
Temperature dependence V_{ref} 0 °C ≤ T ≤ 80 °C	<1 mV (trimmed)
	-0.1 mV/°C to +0.2 mV/°C (untrimmed)
Reference voltage sensitivity to DC supply voltage variation:	3.3 mV/V
Fluctuations of V_{ref} caused by X-ray irradiation up to 44 Mrad - MOS transistors: standard layout - DTMOS transistors: ELT	± 6 mV (about 3%)
Fluctuations of V_{ref} caused by X-ray irradiation up to 44 Mrad - MOS transistors: ELT - DTMOS transistors: ELT	±1.5 mV (about 0.8%)

value differs from chip to chip and is caused by process variations. Based on measurements on a small number of (unselected) samples, the quadratic mean value of statistical spread of the reference voltage has been estimated as low as 6 mV.

According to Monte-Carlo simulations in Cadence, process variation of the threshold voltage of DTMOST devices is the major cause of the spread of the reference voltage.

VIII. CONCLUSIONS

A new radiation hard bandgap voltage reference circuit has been designed in a standard triple-well 0.13 μm CMOS technology. The main cause of the radiation sensitivity in conventional bandgap reference circuit is in charging of field oxide in a conventional diode, yielding up to 4% voltage change for irradiation up to 79 Mrad. In the presented design DTMOST diodes were used which are inherently tolerant to radiation, yielding up to 0.8% voltage change at 40 Mrad.

The measured specifications of the design are given in Table I.

ACKNOWLEDGMENT

The authors would like to thank P. Moreira and F. Faccio of CERN, Geneva, Switzerland, for cooperation on irradiation of the chips and useful discussions, and J. Rövekamp of Nikhef, Amsterdam, The Netherlands for technical support.

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