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THE CONSEQUENCES OF THE APPLICATION OF A FLOATING GATE ON d.c.-MISFET CHARACTERISTICS

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Abstract—In the literature the influence of the conducting layer, sometimes called a floating gate, upon d.c.-MISFET characteristics is ignored or only treated in a phenomenological way. Our intentions in this paper are to present a study of the consequences of a conducting layer in an exact way by using the MISFET theory described earlier.

It is found that the d.c.-characteristics are influenced by parasitic capacitances from the conducting layer to source and drain and the charge-voltage relations along the channel of the MIS transistor.

The theoretical considerations are verified by simulations with Spice 2 and some experimental results and are in agreement with the characteristics already given in the literature referred to.

NOTATION

A_1	floating gate-insulator interface
A_2	floating gate-insulator interface
C_{gs}	parasitic gate-source capacitance, F
C_{gd}	parasitic gate-drain capacitance, F
$C_{ox}^{\square}$	oxide capacitance per unit area, F/m^2
C_{ox}	actual oxide capacitance, F
I_d	drain current, A
L	channel-length, m
$q_m(x)$	density of mobile charge in the channel, C/m^2
q_{g1}	interface charge density, C/m^2
q_{g2}	interface charge density, C/m^2
$V(x)$	potential in the channel, V
V_d	drain-source voltage, V
V_g	gate-source voltage, V
V_g^*	$V_g - V_T$, V
V_{sat}	saturation voltage, V
V_T	threshold voltage, V
V_{up}	voltage of the upper layer, V
W	channel-width, m
α	ratio of capacitances,
β	$\mu C_{ox}^{\square} W/L$, mA/v^2
γ	ratio of capacitances,
μ	drift mobility in the channel, m^2/Vs
ϕ_f	fermi-potential difference, V
ϕ_{ms}	fermi-potential difference, V

1. INTRODUCTION

In the past, various types of MISFET structures have been presented in the literature. This paper will be especially restricted to those types of MISFETs in which the insulating film consists of two layers, separated by a conducting layer, for instance aluminum or polysilicon.

Examples of this type of device are the MISFET with a floating gate[1], mainly in use as a memory device, the acoustic wave sensing POSFET, investigated by Swartz *et al.*[2], and the ion sensitive field effect transistor, described by Smith *et al.*[3].

A floating gate memory device is characterized by two insulating layers of SiO_2, separated by a polysilicon gate. Memory function is obtained by charge storage on and removal from the floating gate, resulting in drain current variations.

The POSFET is composed of a conventional MOSFET and a second insulator of piezoelectric material, for instance polyvinylidene fluoride (PVF_2). This insulator is covered with a second conducting layer that is connected to an external voltage source or ground. Variations of pressure generates electronic charge that is collected on the gate of the transistor.

The ion-sensitive field effect transistor, mentioned above, is formed by a layer of for instance silicon-nitride, a floating gate of gold, a very high resistive, ion selective membrane and a solution from which the concentration of a specific ion has to be measured. The gold layer protects the FET structure against diffusion of ions or water.

In the literature already mentioned, a functional description of the different devices is given, but the influence of the floating gate on the device characteristics is treated only phenomenologically in less detail. This paper reports the results of the study of these devices and the consequences of a floating gate upon the d.c.-transistor characteristics in a more exact way. Although the purposes for which the described types of devices have been developed differ widely, they are conceptually the same. Therefore the configuration as schematically drawn in Fig. 1 can be used in our considerations for all cases.

We shall use the coordinate system as given in Fig. 1, with the x-axis along the channel, x equal to zero at the source-channel interface and the y-axis perpendicular to the surface.

All further descriptions will be given for p-type silicon, n-channel depletion type MOSFETs, assuming that the insulating layers are homogeneous and plan-parallel to the silicon surface, with the bulk connected to the source.

In contradiction to the normal use of a floating gate memory device, we will assume that the insulators are perfect and the floating gate is electrically uncharged.

We define the conducting layer between the two insulators as the gate with voltage V_g with respect to the source. The second conductor that covers the whole configuration is called the upper layer with voltage V_{up} with respect to the source.

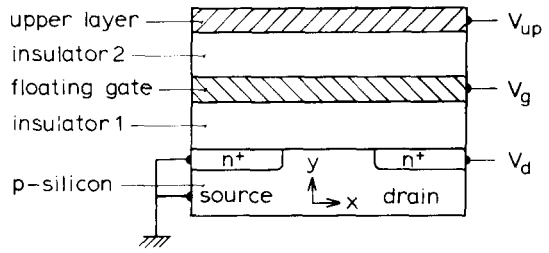

Fig. 1. Cross section of a floating gate structure.

Floating gate memory devices are not covered with a conducting upper layer which corresponds to an infinite thickness of the second insulator. By varying the thickness of the second insulator the transistor characteristics will change and thus this thickness can be used as a parameter in calculating these characteristics. It will be clear that in the absence of the floating gate, a conventional MOSFET with a sandwich insulator results, with its gate identical to the upper layer.

2. MOS TRANSISTOR THEORY

The operation of the MOS transistor is well known and has been described extensively in the literature, see for instance[4, 5].

In a first order approximation bulk effects are neglected and the density of mobile charge in the channel can be written as:

$$q_m(x) = -C_{ox}^{\square}(V_g - V_T - V(x)) \tag{1}$$

with $C_{ox}^{\square}$ the oxide capacitance per unit area, V_T the threshold or turn on voltage, $V(x)$ the potential in the channel at location x with respect to the source voltage, and V_g the applied gate-source voltage.

The drain current I_d can now be written as a function of the applied voltages as follows:

$$I_d = \beta\left[(V_g - V_T)V_d - \frac{1}{2}V_d^2\right] \tag{2}$$

with $\beta = \mu W/L.C_{ox}^{\square}$, V_d the drain-source voltage, μ the mobility of charge carriers in the channel and W and L the width and length of the channel respectively. Note, that for depletion type transistors, as we consider here, $V_T < 0$. The value of V_d for which the mobile charge density in the channel $q_m(x)$ equals zero, just at the drain-channel interface can be found by using eqn (1) and realizing that $V(L) = V_d$. This value of V_d is called the saturation voltage V_{sat} and is given by:

$$V_{sat} = V_g - V_T. \tag{3}$$

According to eqn (2) the drain current then reaches its maximum value. For larger values of V_d relation (2) will no longer be valid and the drain current is then given by:

$$I_d = \frac{1}{2}\beta(V_g - V_T)^2 = \frac{1}{2}\beta V_{sat}^2 \tag{4}$$

and thus no longer depends on the drain to source voltage V_d.

3. THE FLOATING GATE STRUCTURE

We shall now deal in more detail with the floating gate structure, as given in Fig. 2. The parasitic gate-to-source and gate-to-drain capacitances are noted as C_{gs} and C_{gd} respectively, the capacitance formed by the two conducting layers and insulator 2 as C_{up}, while the actual oxide capacitance is C_{ox}, with $C_{ox} = W.L.C_{ox}^{\square}$.

Parasitic capacitances are always present in the practical cases as mentioned in the introduction. The sensitivity of the POSFET configuration was strongly influenced by the presence of a very large gate-to-source capacitance. Even in conventional MOSFET fabrication these capacitances are inevitable.

To simplify further descriptions we now distinguish between the situation in which parasitic gate capacitances are much larger than the actual oxide capacitance C_{ox}, and the situation in which parasitic capacitances are absent.

(a) *A floating gate with large parasitic capacitances*

If the parasitic capacitances are much larger than the actual oxide capacitance C_{ox}, we can ignore the influence of the latter without making a large error.

By applying a voltage V_{up} to the upper plate with respect to the source and realizing the floating gate to be electrically uncharged, the gate-to-source voltage V_g is totally determined by the applied voltages and the capacitances C_{gs}, C_{gd} and C_{up}. We can write:

$$V_g = \frac{C_{gd}V_d + C_{up}V_{up}}{C_{gs} + C_{gd} + C_{up}}. \tag{5}$$

If the upper plate voltage is equal to zero, we can write the drain current I_d as a function of the drain-to-source voltage, by using relations (2) and (5):

$$I_d = \beta\left[(\alpha V_d - V_T)V_d - \frac{1}{2}V_d^2\right] \tag{6}$$

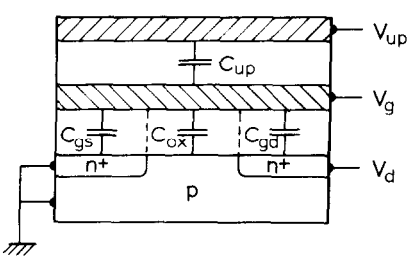

Fig. 2. Capacitances in a floating gate structure.

with $\alpha = C_{gd}/(C_{gd} + C_{gs} + C_{up})$, always positive and smaller than unity.

The value of V_d for which the channel is pinched off, just at the drain-channel interface, can be found in a way, analogous to considerations for conventional MOSFET theory as given in eqns (1–4), and we then obtain:

$$V^*_{sat} = -V_T/(1-\alpha). \tag{7}$$

In normal saturated MOSFET operation the drain current is independent of drain-to-source voltage variations, see eqn (4), but in the case of a floating gate with large parasitic capacitances the gate-to-source voltage always depends on V_d and for the saturated drain current we have to write:

$$I_d = \beta\left[(\alpha V_d - V_T)V^*_{sat} - \frac{1}{2}V^{*2}_{sat}\right]. \tag{8}$$

For n-channel depletion type transistors the threshold voltage will be negative, and thus V^*_{sat} will always be positive. The I_d–V_d characteristics for V_{up} equal to zero and several values of α are calculated and given in Fig. 3, with $V_T = -3$ V, and $\beta = 1$ mA/V^2.

The characteristics are strongly dependent on the value of α. If α equals zero, normal MOSFET characteristics with $V_g = 0$ result, while for $\alpha = 0.5$ a linear characteristic is obtained. Note that in this case the drain current is a linear function of V_d for all values, although the device is operating in the saturated region if $V_d > V^*_{sat} = -2V_T$.

(b) *A floating gate without parasitic capacitances*

In this case we assume no parasitic capacitances are present. Therefore we can no longer neglect the influence of the actual oxide capacitance C_{ox}. If we assume C_{ox} to be equally divided into a gate-to-source and a gate-to-drain capacitance, then no essential differences with the previously discussed situation can be expected. This case would behave as the curve with $\alpha = 0.5$ in Fig. 3.

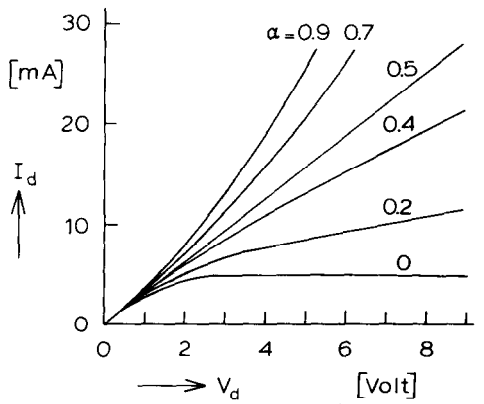

Fig. 3. Calculated I_d–V_d characteristics if parasitic capacitances are dominating, with α as a parameter, $V_{up} = 0$ V, $V_T = -3$ V and $\beta = 1$ mA/V^2.

In the following consideration however we shall explain that such a symmetrical division introduces unacceptable errors for increasing values of the drain-source voltage V_d.

The expression for the charge density per unit area q_{g1}, at the floating gate-insulator 1 interface can easily be derived from the MOSFET theory already known:

$$q_{g1} = C_{ox}{}^{\square}[V_g - \phi_{ms} - 2\phi_f - V(x)] \tag{9}$$

with ϕ_{ms} the difference in contact potential between the metal of the floating gate and the doped silicon, and ϕ_f the difference in fermi potential between the doped bulk silicon and intrinsic silicon.

At the floating gate-insulator 2 interface the charge density q_{g2} per unit area equals:

$$q_{g2} = C_{up}{}^{\square}[V_g - V_{up}] \tag{10}$$

with $C_{up}{}^{\square} = C_{up}/(W.L)$, assuming the upper layer and the floating gate to be of equal size and shape.

In the unsaturated mode the potential $V(x)$ in the channel can be written as a function of V_d, V_g and V_T, by substituting in eqn (2) $V(x)$ for V_d and x for L:

$$V(x) = V^*_g - \left[V^{*2}_g - (2V^*_g - V^2_d)\frac{x}{L}\right]^{1/2} \tag{11}$$

where $V^*_g = V_g - V_T$.

Although local charge densities at the floating gate insulator interfaces can be present, we assumed the floating gate to be electrically uncharged, and thus:

$$\int_{A_1} q_{g1}\,dA + \int_{A_2} q_{g2}\,dA = 0 \tag{12}$$

with A_1 and A_2 the floating gate-insulator 1 and -insulator 2 surface respectively.

By combining eqns (9–12) we obtain an implicit expression for the gate-to-source voltage, which can be simplified to a relation similar to eqn (5):

$$V_g = \frac{\phi_{ms} + 2\phi_f + \gamma \cdot V_{up} + V_d(2V_d - 3V^*_g)/(3V_d - 6V^*_g)}{1+\gamma} \tag{13}$$

with $\gamma = C_{up}/C_{ox} = C_{up}{}^{\square}/C_{ox}{}^{\square}$.

By rearranging relation (13) a second-order expression for V_g is obtained, and thus the I_d–V_d characteristics with γ as a parameter can be calculated. Results for $V_{up} = 0$, $V_T = -3$ V, $\phi_{ms} + 2\phi_f = -0.4$ V and $\beta = 1$ mA/V^2 are given in Fig. 4.

Zero thickness of the second insulator results in a conventional MOSFET and relation (13) is reduced to $V_g = V_{up}$, because γ becomes infinite. In the saturated mode of operation the potential $V(x)$ along the channel no longer depends on V_d and thus V_g as well as the drain current I_d become constant.

It is not our purpose to discuss the a.c.-characteristics of the floating gate structure, but

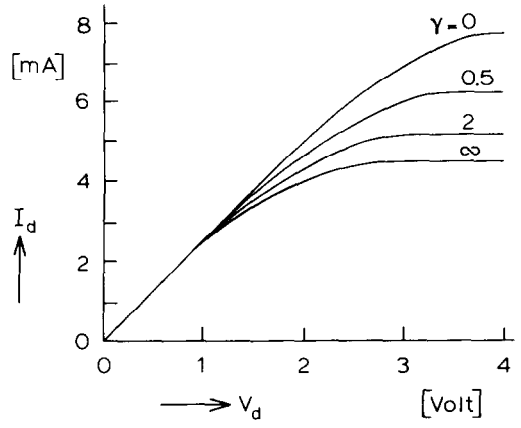

Fig. 4. Calculated I_d–V_d characteristics if parasitic capacitances are absent, with γ as a parameter, $V_{up} = 0$, $V_T = -3$ V and $\beta = 1$ mA/V^2.

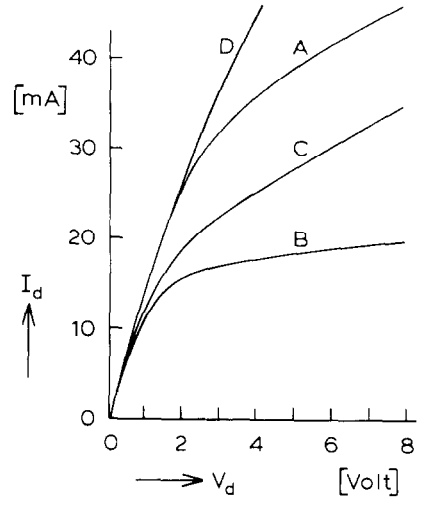

Fig. 5. Experimental I_d–V_d characteristics with A: floating gate, B: $V_g = 0$, C: $V_g = 0.15\ V_d$ and D: $V_g = 0.5\ V_d$.

the explained d.c.-behaviour can be shown to be in good agreement with already known a.c.-MOSFET features.

The last term of relation (13) equals $0.5\ V_d/(1+\gamma)$ for small values of V_d with respect to V_g^*. This dependence of V_g on V_d can be obtained also if we assume the actual oxide capacitance C_{ox} to be equally divided into a gate-to-source and a gate-to-drain capacitance.

The relation between V_g and V_d, that can be derived from eqn (13), however, is no longer linear, which is in agreement with the already known dependence of the differential gate-to-source and gate-to-drain capacitance of a conventional MOSFET on the applied voltages[6, 7].

In the saturated mode the differential gate-to-drain capacitance of a conventional MOSFET becomes zero, which corresponds to the case that V_g is independent of V_d.

4. EXPERIMENTAL

In the practical situation the first discussed case with dominating parasitic capacitances can be avoided as much as possible by optimizing the device fabrication process.

The second mentioned case without effective parasitic capacitances will never be reached because bonding wires and package leads easily introduce parasitic capacitances in the same order of magnitude as the total oxide capacitance C_{ox}. Measured I_d–V_d characteristics will therefore always be a combination of the theoretical curves given in the Figs. 3 and 4.

To verify the calculated results we have measured the I_d–V_d characteristics of MOSFETs with unconnected gate of the type Philips–BFR 29. Results are given in Fig. 5, curve A.

In the same figure the curves B, C and D are shown with $V_g = 0$, $V_g = 0.15\ V_d$ and $V_g = 0.5\ V_d$ respectively, to be able to explain the floating gate characteristic.

The ratios between V_g and V_d are realized by connecting different resistors between the gate-, drain- and source-terminals, simulating well defined capacitances.

For small values of the drain-source voltage, curve A behaves like curve D with $V_g = 0.5\ V_d$. The floating gate characteristic differs more and more from curve D for increasing values of V_d, and for very large drain-source voltages the slopes of curve A and C with $V_g = 0.15\ V_d$ are nearly the same.

Curve A can thus not be described with a constant ratio between V_g and V_d, and also does not fit to one of the curves given in Fig. 4.

Therefore we conclude that the gate-source and gate-drain capacitance are neither very large with respect to the actual oxide capacitance, nor equal to zero. The experimental curve can not be explained by one of the two extreme cases.

Although the measured curve A can be explained qualitatively, we have to combine the theories, given for the two extreme situations to describe the total curve in an exact way. This however, will result in an equation much more complicated than relation (13).

Hence, it is more useful to compare the measured device characteristics with simulated results. For this purpose we have used the Spice 2 simulation program, developed at University of California, Berkeley, U.S.A.

First of all we have chosen realistic values for the channel length L, the channel width W, the oxide capacitance per unit area $C_{ox}^{\square}$, and the threshold voltage V_T of the Philips–BFR 29.

The drift mobility of carriers in the channel μ, and the substrate doping N_{sub} are varied to obtain a simulated curve maximally fitted to the measured curve B of Fig. 5. In this way we determined: $L = 10\ \mu m$, $W = 5200\ \mu m$, $C_{ox}^{\square} = 1.7 \cdot 10^{-4}$ F/m^2, $V_T = -3$ V, $\mu = 600$ cm^2/Vs and $N_{sub} = 1.8 \cdot 10^{15}$ cm^3.

All other parameters used in the Spice simulation are chosen large or small, to be of negligible influence

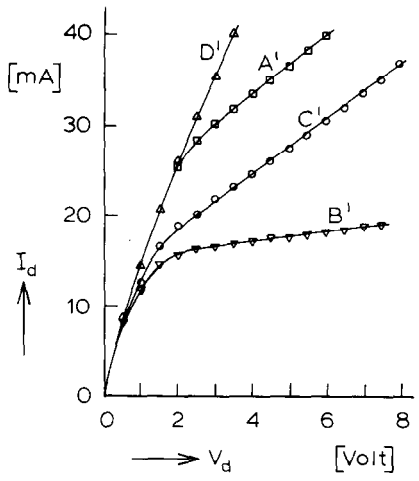

Fig. 6. Simulated I_d–V_d characteristics with A': $C_{gd} = 1$ pF and $C_{gs} = 0$ pF, B': $V_g = 0$, C': $V_g = 0.15\ V_d$ and D': $V_g = 0.5\ V_d$.

on the performance of the characteristics. The corresponding value of the actual oxide capacitance C_{ox} is 8.9 pF.

In our calculations the voltage V_{up} of the upper plate is supposed to be equal to zero. The capacitances C_{up} and C_{gs} are thus connected in parallel and therefore can be considered as one capacitance C_{gs} between gate and source.

In the Spice simulation program leakage resistors between gate-, drain- and source-terminals must have finite values.

These resistors introduce, together with the capacitances C_{gs}, C_{gd} and C_{ox}, a time constant in the order of seconds. To simulate the d.c. I_d–V_d characteristics we therefore have used a transient analysis. Results of the simulation are shown in Fig. 6. The parasitic capacitances C_{gs} and C_{gd}, as given in Fig. 2, are simulated by external capacitances, connected between the drain-gate, and source-terminals. The drain-source voltage V_d is increased with 0.1 V/μsec.

Curve C' is obtained with $C_{gd} = 100$ pF, and $C_{gs} = 560$ pF, and curve D' with $C_{gd} = 100$ pF and $C_{gs} = 100$ pF. Curve A' of Fig. 6 is fitted to curve A of Fig. 5 by varying the values of the capacitances C_{gs} and C_{gd}.

The simulations are strongly influenced by the value of the gate to drain capacitance and are rather insensitive to variations of the gate to source capacitance. Curve A', shown in Fig. 6 is obtained with $C_{gd} = 1$ pF and C_{gs} equal to zero. The error of the simulated results is always less than 8% with respect tot he measured results, which is sufficiently accurate for our purpose.

5. CONCLUSIONS

By using first order MOSFET theory the influence of a floating gate on d.c.-MISFET characteristics can be described in an exact way for two extreme situations. In the first case parasitic capacitances are dominating, in the second they are equal to zero.

The description for all other cases will lead to rather complicated equations, but the characteristics can easily be calculated by the Spice 2 simulation program.

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