

INTEGRATED CASCADE OF PHOTOVOLTAIC CELLS AS A POWER SUPPLY FOR INTEGRATED CIRCUITS

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Abstract

ICs can be powered directly by light when a supply voltage source capable of generating a multiple of the open circuit voltage of one pn-junction is available on a chip. Two schemes have been investigated for cascading photovoltaic cells on the chip. The structures can be made compatible with standard bipolar processes. Deep ion implantations have been used here to realize the multiple-junction structure. Power losses due to photocurrents originating from insulation junctions in the cascade can be kept to a minimum. The surface areas of two adjacent cells have to satisfy a definite relation to ensure the build-up of output voltage. Operating under sunlight conditions, 0.6 mW/cm^2 has been generated in a cascade of three cells. With appropriate optical coatings on the silicon surface and optimized cell dimensions, it should be possible to generate a few milliwatts per cm^2 . The structures may have applications in electronic circuits for glass fibres or can be used to power small CMOS circuits.

Introduction

There are several conceivable situations where light could be used advantageously to power integrated circuits, if a few volts output voltage is generated. Signal processing circuitry could be integrated together with a light sensor to generate T²L-compatible voltages. In combination with I²L, where light can generate gate current directly [1], a voltage source with a somewhat larger output voltage than one diode-drop could power interface circuits.

A single photovoltaic cell will use the bulk of the chip as one terminal of the device. Insulating junctions that have to be reverse biased are necessary to connect cells in series. Since these junctions are also unavoidably irradiated with light, special measures will have to be taken to prevent the generated photocurrent from forward biasing the junctions. At the same time a transistor is created that could jeopardize the intended build-up of output voltage. Two schemes where these potential problems are prevented

have been realized, and are presented here. The device structure in the schemes is such that the process can be made compatible with standard bipolar processes. Ion implantation is used here to show the feasibility of a fully-implanted bipolar process, where deep implantations (1 MeV) are used to avoid epiwafers.

However, a classical bipolar process would have the advantage of junctions appearing at a greater depth, thus increasing the collection efficiency of generated carriers.

A realistic requirement of a power source is that even when used for small circuits, close to a milliwatt should be produced. In sunlight conditions, with a good optical coating, a single photovoltaic cell generates 30 - 35 mA/cm² with an open circuit voltage of the order of 0.55 V, hence several mW/cm² are generated. If we aim at chip sizes smaller than 1 cm², then we conclude that the power loss due to cascading of the cells has to be kept well under control.

A Two-junction structure

The most straightforward realization of a cascade is shown in Fig. 1.

The top np-junction will collect generated carriers from just under the silicon surface to roughly half way down the p-layer (depending on the recombination velocity at the Si-SiO₂ interface and the ratio of voltages across the two pn-junctions), and the bottom junction will collect generated carriers from the bottom half of the p-layer, and from the bulk within the diffusion length from the junction. The bulk is the reference electrode and the top np-junction generates the output photocurrent and photovoltage. The lower junction takes care of the insulation of the cells and has to be reverse biased (or zero biased in the case of the first cell). Kirchoff's current law can be applied to node A in the equivalent circuit diagram (Fig. 1(b)).

$$I_{out_1} = I_{L1} + I_{L2} - (1 - \alpha_d)I_1 - (1 - \alpha_{up})I_2 \tag{1}$$

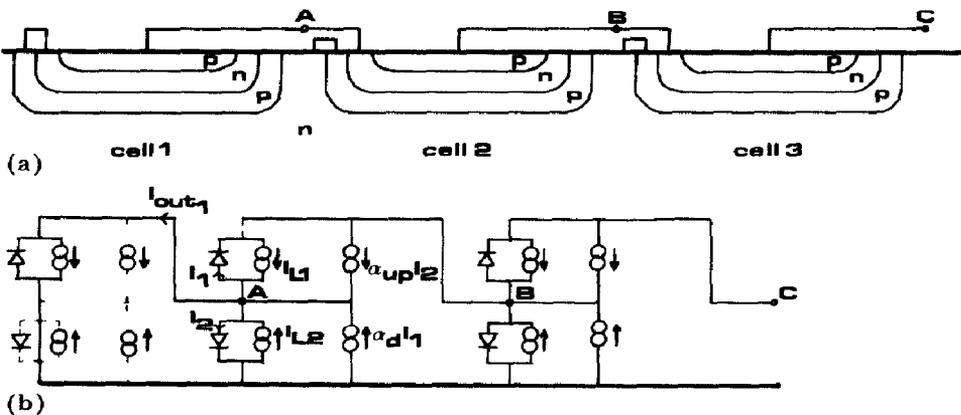


Fig. 1 (a) Cascade of photocells in the two-junction structure, (b) the network equivalent of the structure, showing the d.c. Ebers-Moll equivalent of the transistors.

where $I_{L1,2}$ are the generated photocurrents, and $I_{1,2}$ the transistor currents I_{out} is the output current of the cell, and α_d and α_{up} are the emitter efficiencies of the downward and upward transistors respectively

The condition of reverse bias for the insulation junction requires $I_2 \approx 0$, so at least

$$I_{out_i} > I_{L1} + I_{L2} - (1 - \alpha_d)I_1 \quad (2)$$

This condition should be satisfied for all operating conditions of cell 2, the severest being short circuiting cell 2, when $I_1 = 0$. The maximum output current of cell 2 is I_{L1} . I_{L2} is a loss current.

Condition (2) can, *mutatis mutandis*, also be derived for node B, and when we introduce a loss current ratio, $\epsilon_{21} = I_{L2}/I_{L1}$, condition (2) can be transformed into a condition for the ratio of surface areas of two adjacent cells in the cascade, since

$$(I_{L1} + \epsilon_{21}I_{L1})_{i+1} < I_{out_i} \leq (I_{L1})_i$$

or

$$A_{i+1}/A_i > 1/1 + \epsilon_{21} \quad (3)$$

where the indices i and $i + 1$ refer to cell numbers, and A is the surface area.

For all cells in the cascade, the bottom junction generates a loss current. For a correct comparison of the power efficiency of a cascade of i cells to that of one photovoltaic cell, we can relate the available power per unit surface area of an i -cell cascade, p_i , to the total available power per unit surface of both junctions, $p_1 + p_2$, of one cell as

$$\frac{p_i}{p_1 + p_2} < \frac{i}{(1 + \epsilon_{21})^i + \dots + (1 + \epsilon_{21})} \quad (4)$$

The analysis of the role of the parasitic transistors is simplified when condition (2) is observed. The bulk p-junction will not behave as an emitter-base junction of an upward transistor, so only the downward npn transistor will operate in the normal mode. The effect of this transistor is that electrons coming from the top n-layer will diffuse through the p-layer to the bulk, instead of recombining in the p-layer. This has no effect on the output current of the cell, nor on the voltage across the top np-junction. The operation of the scheme is independent of the current amplification factors of the transistor, and it can thus be implemented in any bipolar process.

It must be noted, however, that the sheet resistances of the buried layers must be kept as low as possible. For the implantation profile of Fig 5, which is (except for the top p-layer) the profile used for this structure, the bottom p-layer has a sheet resistance of $\approx 1 \text{ k}\Omega/\square$. When low resistive contacts are made on all four sides of the buried layer, lateral currents will not be large enough to establish voltage drops that effectively forward bias the bottom junction, and thus would reduce the output voltage of the cell.

Realization and results

Figure 2 shows a chip photograph and I - V characteristics of a series connection of three cells operated under low intensity TL irradiation. For this condition, the loss current ratio, ϵ_{21} , was measured to be 0.8. In direct sunlight this ratio was 3, indicating the presence of intense long wavelength radiation. Sunlight filtered through a blue filter yields a small loss current ratio $\epsilon_{21} = 0.2$, so the two-junction structure will be most effective when short wavelength light is used. The buried p-layer was made using a 1 MeV boron implantation with a peak concentration of 10^{18} cm^{-3} at $1.6 \mu\text{m}$ from the surface. The top n-layer is diffused from a phosphorus-doped oxide to give a high surface concentration for an ohmic contact.

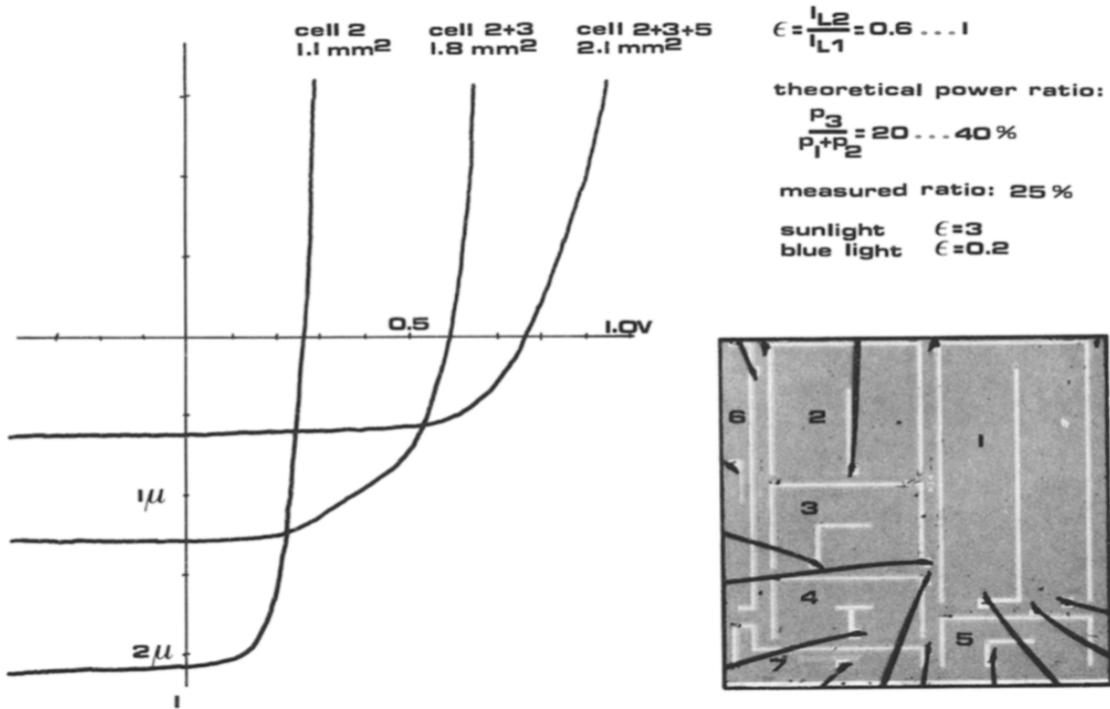


Fig. 2. Chip photograph and I - V characteristics under low-intensity TL irradiation.

B. Three-junction structure

To minimize the loss current ratio, the collecting range of the loss diode can be reduced by adding an extra junction under the insulating junction. A three-junction device is now obtained, as shown in Fig. 3.

In fact a p-layer is introduced on top, which permits us to remain on an n-substrate. Output currents and voltage now have opposite signs compared to those of the two-junction structure.

Since the creation of a deep n-type layer with ion implantation requires very high accelerating voltages, a pnp structure has been chosen, but in

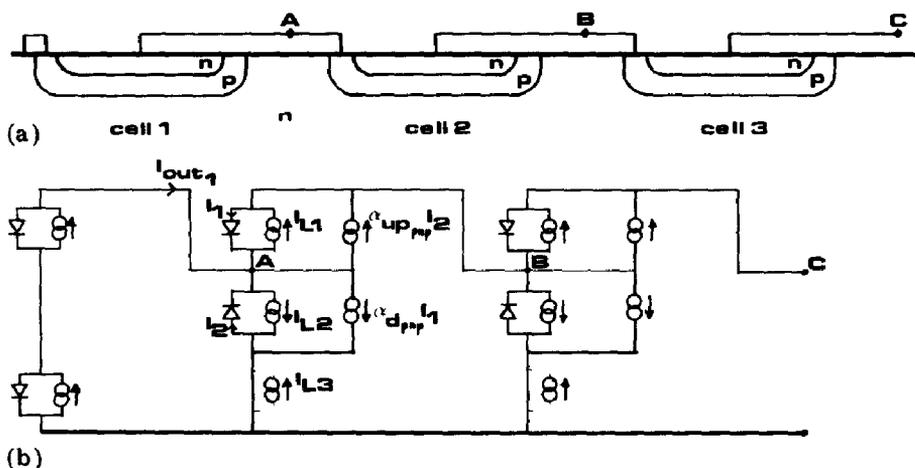


Fig 3 (a) Three-junction device with reduced loss Two junctions of the first cell are connected in series, further cells have their bottom junction shortened (b) Circuit equivalent showing only the active junctions

principle npn structures can also be used, of course Condition (2) can still be applied to node A, but since junction 2 collects generated minorities from a smaller depth in the silicon and hence will show a small photocurrent, the surface areas of two adjacent cells can be nearly equal

A different power efficiency will now result, since the bottom junction from the first cell is also used

$$\frac{p_i}{p_1 + p_2 + p_3} < \frac{(t + 1)/(1 + \epsilon_{21} + \epsilon_{31})}{1 + (1 + \epsilon_{21}) + (1 + \epsilon_{21})^{t-1}} \quad (5)$$

where $\epsilon_{31} = I_{L3}/I_{L1}$ The series connection of the bottom and top junctions in the first cell is only possible when $I_{L3} > I_{L1}$ When this is not the case, both bottom junctions of cell 1 have to be shortened and the power efficiency reduces to

$$\frac{p_i}{p_1 + p_2 + p_3} < \frac{t/(1 + \epsilon_{21} + \epsilon_{31})}{1 + (1 + \epsilon_{21}) + (1 + \epsilon_{21})^{t-1}} \quad (6)$$

The role of the parasitic transistors can be analysed relatively simply when the operating conditions of the cascade are again observed Only downward transistors are active, which will not affect the output capabilities of the structure This flexibility allows adaptation of the process to other bipolar processes

Realization and results

Figure 4 shows a chip photograph and $I-V$ curves of three series-connected cells, operated at low-intensity TL irradiation The small output current of cell 4 is caused by its small size compared to cell 3 Cell 4 could have been made larger, while still satisfying the operating conditions of the cascade Under the same light conditions as for the two-junction structure,

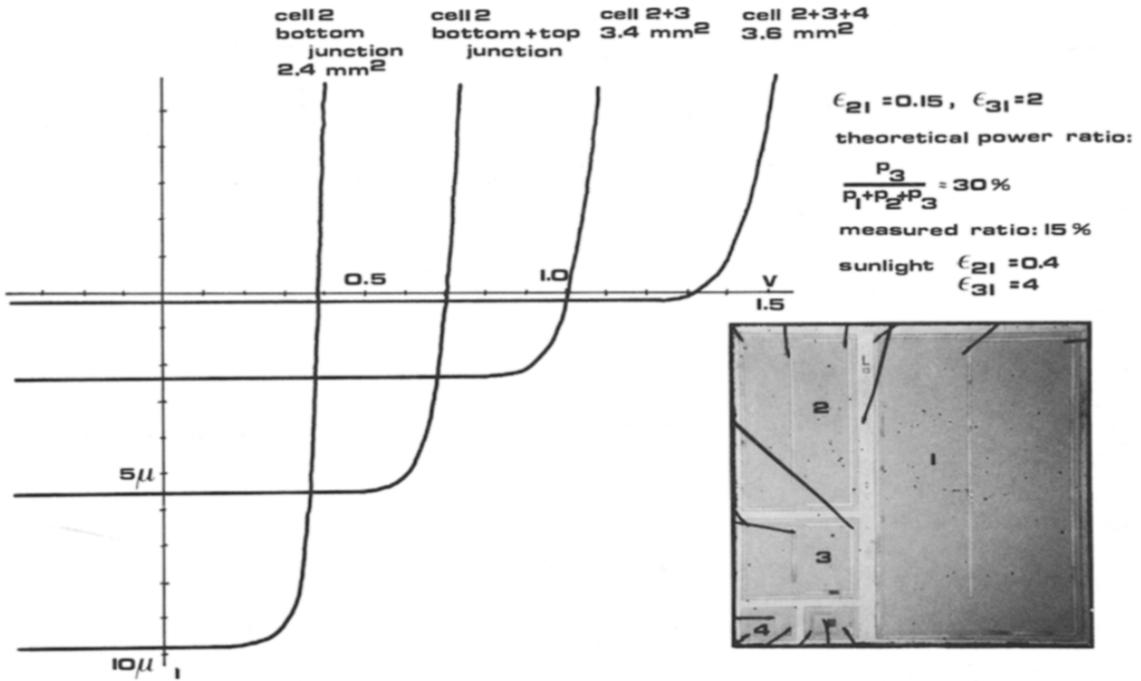


Fig 4 Chip photograph of three-junction structures and I - V characteristics of the cascade

the loss ratio $\epsilon_{21} = 0.15$, i.e., it is five times smaller. The bottom junction loss, $\epsilon_{31} = 2$, is larger than ϵ_{21} of the two-junction structure because of the reduced collection depth of the top junction due to the implantation of the extra p-layer.

With the three largest cells of the chip cascaded and irradiated with direct sunlight, an output voltage of 1.53 V and short-circuit current of 45 μ A were produced. The total surface area of the cascade was 11 mm², and no special coating on the chip surface was applied. It is reasonable to expect that this result of 0.6 mW/cm² can be improved significantly when the device is optimized for the sunlight spectrum.

The impurity profile of the realized structure is as in Fig 5. Only one 15 minute anneal at 900 °C is applied to activate the impurities and remove the damage. Junction leakage currents smaller than 50 nA/cm² were obtained. To enhance the collection efficiency of the top junction, a built-in electric field could be established by creating a gradient in the top boron implantation.

Discussion

The output power available from a photovoltaic cell depends on the collection efficiency of generated minorities at the junction, and on the value of the reverse saturation current of the diode.

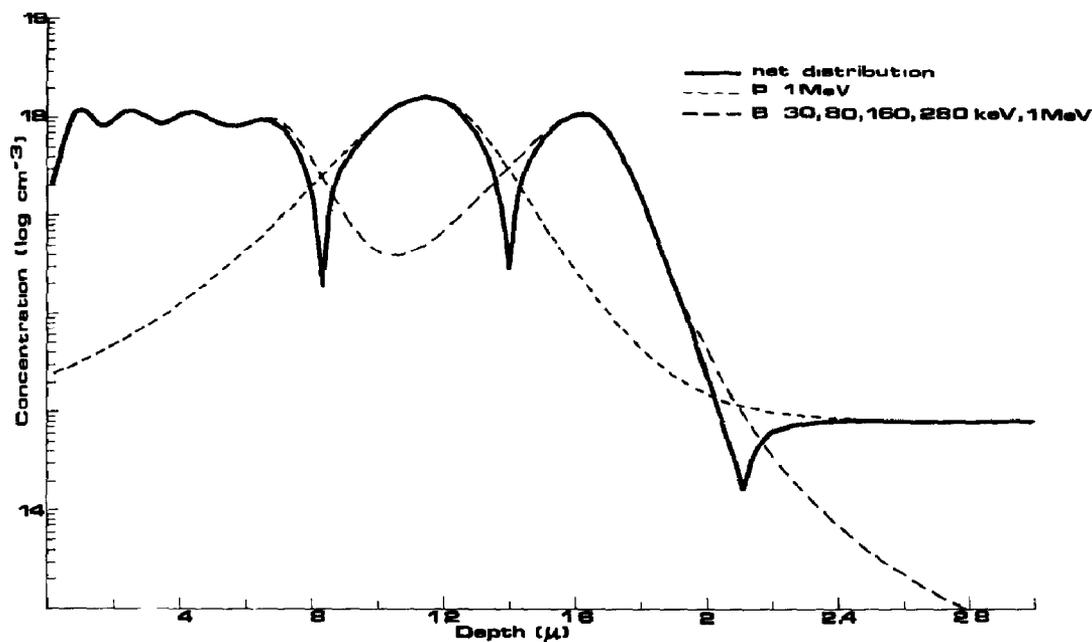


Fig 5 Impurity profile of the three-junction device

The collection efficiency can be optimized by, *e g*, adjusting the depth of the junction. The lifetimes of minorities at both sides of the junction should be made as large as possible, which means that doping concentrations should be kept low. A small reverse leakage current, however, requires high doping concentrations and large diffusion lengths, and/or widely spaced junctions.

The two-junction structure will be particularly suitable for short-wavelength light, since only then can a low loss ratio be obtained. The operating conditions for the three-junction structure are less critical, the loss ratio ϵ_{21} is low for all light frequencies, but the bottom junction of the first cell requires some long-wavelength light in order to generate enough current to drive the top junction.

Since condition (3) is the only condition that always has to be satisfied, the device structure can be chosen such that doping profiles and junction depths are optimum for the application concerned.

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Biography

Ton Mouthaan received his bachelor degree in electrical engineering from Twente University of Technology in 1974 and his 'Ingenieurs' degree in 1977. After a short period as research affiliate at Twente, working on piezoelectrics, he was employed as lecturer at the University of Zambia in the Electrical Engineering department. Since 1982 he has worked on the applications of deep ion implantations in the Solid State Electronics Group at the Twente University of Technology.