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Low-Cost, Large-Area, Facile, and Rapid Fabrication of Aligned ZnO Nanowire Device Arrays

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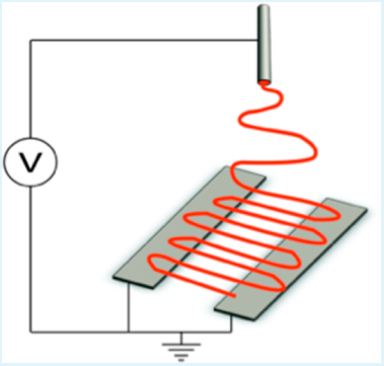
Supporting Information

ABSTRACT: Well aligned nanowires of ZnO have been made with an electrospinning technique using zinc acetate precursor solutions. Employment of two connected parallel collector plates with a separating gap of 4 cm resulted in a very high degree of nanowire alignment. By adjusting the process parameters, the deposition density of the wires could be controlled. Field effect transistors were prepared by depositing wires between two gold electrodes on top of a heavily doped Si substrate covered with a 300 nm oxide layer. These devices showed good FET characteristics and photosensitivity under UV-illumination. The method provides a fast and scalable fabrication route for functional nanowire arrays with a high degree of alignment and control over nanowire spacing.



KEYWORDS: *nanowires, alignment, electrospinning, field effect transistor, UV-detector*

INTRODUCTION

Nanowires of inorganic materials have attracted huge interest over the past decade because of their wide range of applications in the areas of electronics, optoelectronics and sensing. Among other synthesis methods, electrospinning has evolved as an excellent tool for large scale, low cost and relatively fast manufacturing of nanofibers and nanowires over the past decade. Nanowires of a wide range of functional materials, both polymeric and ceramic, have been fabricated by electrospinning and have found application in human tissue engineering,[1] energy storage devices,[2] and sensing.[3] Usually these nanowires are formed as mats of nonoriented ultralong fibers/wires. For the aforementioned applications, alignment is not relevant. However, for the manufacture of low cost electronic, optoelectronic and sensing device arrays, unidirectional alignment of nanowires is essential. Aligned wires allow easy connection of external electrodes at both ends of all nanowires, facilitating the ease and reproducibility of the fabrication process considerably. The first reports of ceramic nanofibers prepared by electrospinning date back to 2002.[4] One year later, Li et al. reported the fabrication of ceramic arrays of aligned nanowires by electrospinning.[5] Since then, there have been reports of devices based on arrays of electrospun nanowires, such as field effect transistors,[6] mechanical energy harvesters,[7] supercapacitors,[8] photosensors,[9] etc. However, these devices were limited to surface areas of a few square micrometers (~10 μm^2). Although the mechanism of fiber alignment in an electrospinning process has been modeled,[10] only experimental studies without control over nanowire spacing have been reported.[11]

The electrospinning process has certain advantages over common nanowire fabrication methods including vapor−liquid solid (VLS) growth, hydrothermal synthesis, and template assisted electrodeposition, since the latter methods cannot produce nanowires with planar alignment on a device substrate. The VLS growth and hydrothermal synthesis methods yield nanowires grown vertically on a substrate. In the case of template assisted electrodeposition, nanowires are electrodeposited in an anodic alumina or polymeric template, followed by template removal. In order to make planar electronic or sensing devices, one then has to disperse the nanowires in a solution and drop cast on a device substrate to obtain horizontally oriented nanowires. Such device fabrication approaches are time-consuming and only prototype scale devices can be obtained.

In this contribution, we demonstrate that electrospinning can be used as a fast fabrication tool to form large area device arrays of highly aligned ceramic nanowires with a high degree of control over density, shape, and spacing. The process of fabrication of the nanowire devices is shown in Figure 1. Briefly, electrospinning consists of a spinneret connected to a collector counter electrode via a high voltage power supply. When a viscous and moderately conductive precursor solution is

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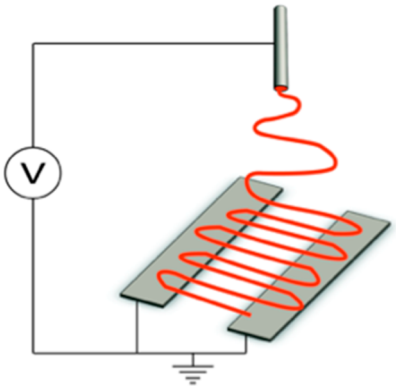

Figure 1. Schematic diagram of the electrospinning process.

pumped into the spinneret, it becomes electrified under the influence of the high voltage and stretches into a nanofiber because of both the electrostatic attraction by the counter electrode and the mutually repulsive electrostatic interactions at the nanofiber surface. The nanofiber dries on its way to the counter electrode where it is collected.[12] A thermal treatment is subsequently applied on these preceramic hybrid wires to convert them into the final metal oxide phase. The method can be used for fast synthesis of aligned oxide nanowire arrays over wafer scale surface areas, and can thus have many potential applications in electronics, optoelectronics, and sensing. The technique can be employed for a wide range of functional oxides. Here, we chose ZnO as a model system to demonstrate the ability of the technique to fabricate large area aligned arrays in a very short period of time and illustrate their applicability by

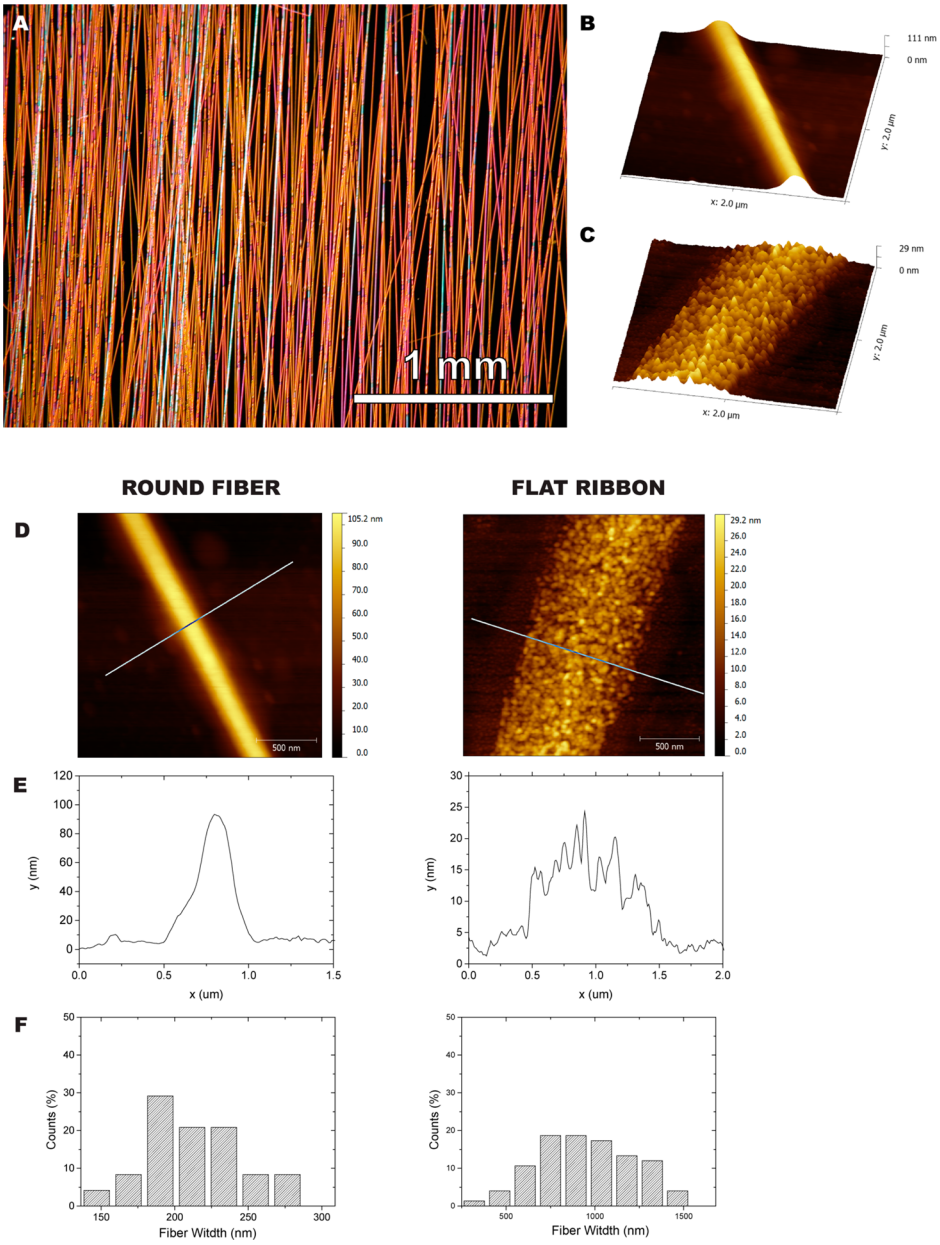

Figure 2. Array of aligned ZnO nanowires. (A) Optical microscope dark field image, in which the reflection of the wires can be seen; (B) 3D AFM topography image of a rounded nanowire; (C) 3D AFM topography of a ribbon-like nanowire; (D) AFM topography scan; (E) height profile extracted from the AFM scan along the line in panel D; and (F) frequency distribution of wire diameter as calculated from SEM images.

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making field effect transistors and photodetector arrays. Aligned electrospun oxide nanowire arrays for photosensors have been demonstrated before,[13,14] but the main advance of our method is that it provides a very fast route with which wafer scale nanowire arrays (4×4 cm^2, see Figure S1) with a high degree of alignment and control over nanowire spacing were obtained, and that is further scalable to industrial scale manufacturing of devices.

EXPERIMENTAL SECTION

Preparation of the Precursor. We prepared a solution of 0.8 M zinc acetate dihydrate (Merck EMSURE ACS) in a 1:1 vol/vol ethanol/water mixture. The solution was heated to 70 °C for complete dissolution. Then, we added 150 mg/mL of polyvinylpyrrolidone (K90, Sigma-Aldrich) (PVP) to the solution and left it stirring for 2 h.

Electrospinning Process. Electrospinning was performed on a homemade setup consisting of a spinneret grounded through a high voltage supply (15 kV) to two metallic collector electrodes forming a gap. A schematic representation of the setup is shown in Figure S2. The distance from the spinneret to the ground electrode was 15 cm. The spinneret had an inner diameter of 0.8 mm. The relative humidity and temperature were kept constant at 30% and 25 °C, respectively. We studied the influence of gap width and deposition time on the alignment and packing of the lines while the flow rate was kept at 0.25 mL/h. We varied the gap between 2.0 and 7.5 cm and the deposition time between single pulse spinning (spinning time <0.5 s, termed "0 s" in the text) and 15 s. To form flat ribbons, the solution was spun at 70 ° C, whereas rounded wires were obtained at room temperature. The samples were annealed in a convection oven at 500 °C in air for 5 h, using a heating/cooling rate of 5 °C/min.

Characterization. Scanning electron microscopy (SEM) imaging was performed with a Zeiss Merlin HR. Atomic force microscopy (AFM) scans were done on a Bruker Icon equipped with a ScanAsyst-Air tip. The imaging of large area arrays of lines was done with a Nikon Eclipse ME600 optical microscope.

Statistical Analysis. The Analysis of variance or ANOVA test is a method used to calculate the difference between more than 2 independent groups of data with normal distribution. The test provides information on the extent to which the data groups have statistically independent results, expressed in terms of the parameter p. Smaller values, that is, $p < 0.001$, indicate statistical differences with a large degree of certainty. The ANOVA test was performed using GraphPad.

Device Fabrication. Electrical contacts were defined on a Si substrate with a thermally grown SiO_2 layer of 285 nm thickness by standard photolithography using a mask aligner (EVG 620 Mask Aligner), followed by metallization by e-beam evaporation (5 nm Ti/65 nm Au at a rate of 0.01 nm/s) and lift-off.

Electrical Transport and Optical Measurements. Electrical measurements were conducted in a home-built probe station under vacuum conditions ($<10^{-5}$ Torr). A Keithley 2643B source meter was used for applying source-drain bias and drain current measurement. A Keithely 2400 source meter was used to apply the voltage. The measurements were performed with an applied gate voltage ranging from −60 to +60 V. To estimate the field effect mobility we used the formula $\mu = [dI_{ds}/dV_g]\cdot(L/WC_iV_{ds})$, where L is the nanowire length and W is the channel width calculated by summing up all nanowire diameters. The capacitance/unit area C_i of the thermally grown SiO_2 gate oxide was estimated to be 1.15×10^{-4} F/m^2, from $C_i = \varepsilon_0\varepsilon_r/d$, where ε_0 is the permittivity of vacuum, $\varepsilon_r = 3.9$ the relative dielectric constant of SiO_2, and $d = 300$ nm. The optical measurement was performed in the same system by illuminating the device with a UV laser (405 nm) with a power density of 2.5 mW/cm^2.

RESULTS AND DISCUSSION

Our method yielded highly aligned nanowires with a length of 4 cm over a large area of 4×4 cm^2 within a processing of time of 15 s. We used two parallel conductive plates with an insulating gap in between as collector in our experiments, so that the wires became aligned by the imposed electric field and electrostatic wire−wire repulsion.[5,10,12,13] We placed the substrates in the electrode gap so that the nanowire arrays would be deposited on them. Our study demonstrates that the spacing between metal oxide nanowires can be controlled by varying the spinning time and the gap length between the two collector electrodes. We used n-type semiconducting zinc oxide (ZnO) as a model system. However, the method can be extended to almost any metal oxide composition that can be made via an electrospinning process. We fabricated a large area field effect transistor (FET) and a UV detector array by aligned electrospinning on top of device substrates with prefabricated electrode arrays. Alternatively, the use of top electrodes which could be fabricated easily on top of nanowire arrays via photolithographic processing is demonstrated.

The electrospinning process described above resulted in large area deposition of highly aligned ZnO nanowires. The dark field optical microscope image in Figure 2a exemplifies this. The reflection of a highly aligned array of wires can be seen. We formed arrays of wires of up to 4 cm in length and width on top of silicon substrates with thermally grown oxide layer of a thickness of 300 nm. To the best of our knowledge, this is the first time that such long fibers and large areas of highly aligned inorganic nanowire arrays are reported.

In general, electrospinning yields nanowires with a circular cross section. When the precursor dried slowly at room temperature after electrospinning, nanowires with a rounded cross section were indeed formed (Figure 2B). After evaporation of the solvents from the fibers, the substrates were annealed at 500 °C to remove the polymeric matrix and crystallize the ZnO phase. The ZnO nanowires formed by this process had an average width of 200 ± 32 nm and a height of about 90 nm (Figure 2D−F). Although the cross-section was not completely circular, it can be seen that the solution at room temperature yielded more rounded fibers than the use of a warm solution (Figure 2C). The flattened fibers were formed by spinning the solution at 70 °C. They had a width of 870 ± 16 nm and a height of 18 ± 3 nm (Figure 2 D−F). The formation of polymeric ribbons by electrospinning has been reported as a consequence of fast drying,[16] which may also be the case here. It was explained by the rapid formation of a solid skin around the wet core of the fibers/wires. Eventually the wires collapse into a ribbon shape upon further drying and shrinkage of their inner parts.[17−20] Flattened wires may actually be beneficial for certain applications, such as sensing, because of the increased surface to volume ratio.

To investigate the control over the nanowire packing density, a matrix of experiments was designed in which the gap width and deposition time were varied. The results are shown in Figure 3. The gap width has a larger effect on nanowire spacing than the deposition time. When different depositions times between 0 (single pulse with duration <0.5 s) and 15 s were compared, the nanowire packings in samples made with gap widths of 2 and 4 cm were the same within experimental error (Figure 3a). The average nanowire spacing was 4.5 μm. In these short experiments, the deposition time had a significant influence on nanowire packing density only at an electrode gap width of 7.5 cm; in that case the wire spacing varied from 239 μm at 0 s to 71 μm after 15 s of deposition.

When samples spun for 15 s with different gap spacings are compared, the samples made using a 2.0 cm gap width did not show optimal alignment (Figure 3b, left). When the gap width

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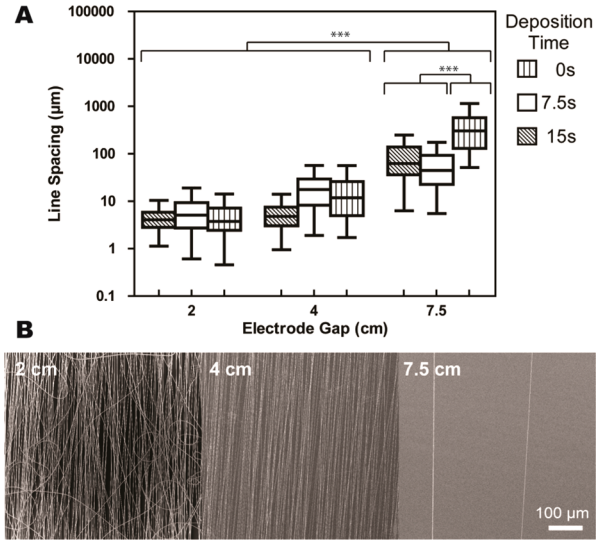

Figure 3. Nanowire spacing. (A) Statistical analysis of samples prepared with different electrode gaps and deposition times. The star signs shows the statistical significance of the difference between samples as calculated by ANOVA tests. The number of stars is a measure of the statistical difference: *** = $p < 0.001$. When no stars are shown the samples are statistically equal. (B) SEM images of samples prepared with gap widths of 2.0, 4.0, and 7.5 cm and pulsed (<0.5 s) deposition.

was increased to 4.0 cm, alignment was improved (Figure 3b, middle). An average spacing of 71 μm, while good alignment was kept (Figure 3b, right). The result suggests a tipping point beyond which the gap width influences wire packing density. The effect may be associated with the nonlinear decrease of the potential at the gap center with increasing gap width, as calculated by Chaurey et al.[15] Their reported model indicates a potential drop between the center of the gap and the edge of the electrode, which causes the wire alignment.

The above results can be understood by considering that wire alignment is electrostatically driven.[12] The electric field lines point toward the metallic electrodes rather than vertically downward,[10,15] that is, a horizontal electrostatic force component is present, especially in and just above the gap. The magnitude of the horizontal component increases with gap width, resulting in improved alignment for wider gaps. The horizontal electrostatic force drags fibers to the electrodes, thus reducing the chance of depositing fibers in the gap. The packing density is therefore a direct measure of the nanowire deposition rate over the gap. The deposition rate is much higher at short gap widths, since the horizontal component of the electric field toward the electrode is much higher and allows the fibers to be deposited on the gap. The influence of long deposition times can only be appreciated at large gap distances since the deposition rate is much smaller than at short gap distances.

To demonstrate the practical applicability of ordered electrospun ZnO nanowires we fabricated field effect transistor (FET) arrays and ultraviolet (UV) detector arrays. Aligned nanowires were electrospun on top of heavily doped Si substrates with a thermally grown oxide layer of 300 nm. We used both top and bottom contact source and drain electrode arrays. For bottom contact devices, we fabricated an array of Ti (2 nm)/Au (60 nm) source-drain electrodes by a photolithography and lift-off process. Then nanowires were electrospun aligned across the electrode arrays, followed by annealing at 500 °C for 2 h in air to crystallize ZnO and obtain device arrays. We have used the rounded nanowires for the fabrication of device arrays. The rounded nanowires had closer packed grains compared to the flat ribbons, which yielded semiconducting nanowires. The flat ribbons did not show any field effect in our electrical measurements and behaved as insulating materials, possibly because of the large spacings between the grains which may have resulted in poor charge transfer. For top contact devices, we first electrospun the nanowires on top of a SiO_2/Si substrate, annealed the wires at 500 °C in air for 2 h and then fabricated the source-drain electrodes on top by a photolithography process. In both cases, the electrodes had dimensions of 100 × 100 μm^2 and each electrode was separated by 100 μm from the next one. An array of FETs was thus obtained in which the metal contacts functioned as source-drain electrodes. The thermal SiO_2 layer functioned as the gate dielectric and the Si substrate functioned as back gate electrode (schematically shown in Figure 4a). An optical microscopy

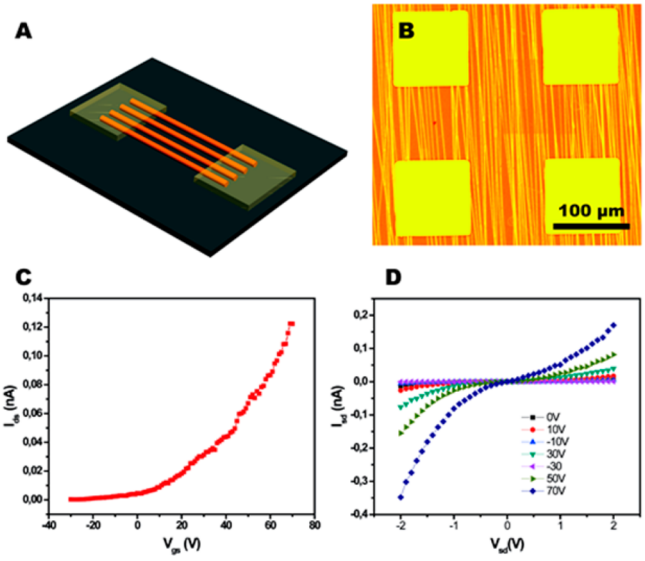

Figure 4. (A) Schematic of electrospun nanowire device. (B) Optical microscopy mage of an electrospun device array. (C) Transfer characteristics of a typical FET (drain current I_{ds} plotted against gate voltage V_G). The drain voltage is 2 V. (D) $I-V$ characteristics of an electrospun ZnO nanowire transistor. The drain current I_{ds} is plotted against the source-drain bias V_{ds} for different gate voltages.

image of the array is shown in Figure 4b. A large area optical micrograph of the device is shown in Figure S3. The same device configuration was used for UV detection. These devices had an average of 16−20 nanowires between the electrodes. Figure 4c shows a typical transfer curve, that is, drain current plotted against gate voltage (I_d-V_g) and in Figure 4d, we show the output drain current−drain voltage ($I_{ds}-V_{ds}$) characteristics of a ZnO nanowire FET with approximately 16−20 nanowires between the source-drain electrodes. The drain current, I_d increased with positive gate voltage showing the n-type behavior of the electrospun ZnO nanowires. The $I_{ds}-V_{ds}$ characteristics showed clear modulation with applied gate voltage. The nanowire FETs had an average mobility of 0.018 $cm^2\ V^{-1}\ s^{-1}$ which is comparable to sol−gel processed ZnO based thin film transistors.[21] Choi et al.[22] have shown that randomly aligned composite (In_2O_3−ZnO−$ZnGa_2O_4$) nanowires can yield high performance FETs with higher field effect mobility (7.04 cm^2). We have used a pure phase of ZnO

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without any doping, which has intrinsically lower mobility values similar to sol−gel processed films. However, any engineered materials which can be processed by electrospinning can be prepared in the form large area highly aligned nanowires by our technique.

A photoconductivity study was also performed on this device. As the nanowires were illuminated with a 2.5 mW/cm^2 405 nm laser, it showed a significant photocurrent (Figure 5, red curve)

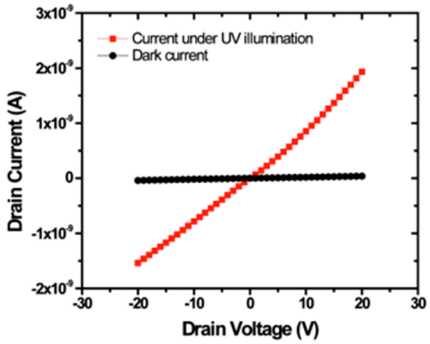

Figure 5. *I*−*V* curve of a ZnO nanowire device with and without UV illumination.

compared with the dark current (black curve). During the measurement, about 20 nanowires with 200 nm diameter were exposed to the laser, so the effective exposure area is 20 × 200 nm × 100 μm = 400 μm^2. The external quantum efficiency of this device is calculated using the equation $\eta = \frac{I_{ph}}{e} \times \frac{E_{ph}}{po} \times 100\%$, where I_{ph} is the difference between current under illumination and dark current, e is the electronic charge, E_{ph} is the photon energy, and po is the incident laser power. The external quantum efficiency was found to be as high as 60%. These device prototypes illustrate the potential applicability of aligned electro-spun nanowire devices for low cost electronic and UV-sensing applications.

CONCLUSIONS

Electrospinning was used to fabricate aligned semiconducting oxide nanowire arrays with 4 cm long wires and a total surface area of 16 cm^2. The nanowire spacing can be controlled by controlling the size of the gap between the electrodes, and to a lesser extent by the deposition time. Aligned nanowire arrays by electrospinning can be used to fabricate low cost large area devices, with control over the nanowire density. Our technique can be extended to many other materials that can be electrospun, such as polymers, organic semiconductors, piezoelectric ceramic nanofibers (Pb(Zr,Ti)O_3, $BaTiO_3$, etc.) and other functional oxides (e.g., SnO_2, CuO, Fe_2O_3, ZnO, ZrO_2, MgO), thus providing a generally applicable platform for nanowire array fabrication for low cost electronic, optoelectronic, sensing and energy devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.6b01594.

Schematic of the electrospinning process, photograph of aligned ZnO nanofibers, and optical micrograph of ZnO nanowire device array (PDF)

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Notes

The authors declare no competing financial interest.

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