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THE MEASUREMENT OF INTERFACE STATE CHARGE IN THE MOS SYSTEM

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Abstract – A simple method of measuring charge in surface states as a function of the surfacepotential in MOS transistors or MOS capacitors is proposed.

A constant d.c. current is fed into the gate of an MOS transistor and with the help of an operational amplifier, the gate voltage V_g with respect to the bulk is plotted as a function of gate charge Q_g. The gate charge as a function of the surfacepotential ϕ_s can be directly read off from the V_g–Q_g curve.

As the silicon charge $Q_s(\phi_s)$ is known from the literature the surface state charge can be easily determined as a function of ϕ_s. The method is illustrated with measurements on *n*-type and *p*-type MOS transistors. Finally the accuracy of the charge measuring method is discussed and a comparison with other interface state charge measuring methods is made from which the charge measuring method evolves as a method, attractive for its simplicity.

Résumé – Une méthode simple pour mesurer la charge d'états de surface en fonction du potentiel de surface ϕ_s dans des transistors MOS ou des condensateurs MOS est proposée.

On charge à courant constant la grille d'un transistor MOS et à l'aide d'un amplificateur opérationnel la tension grille-substrat V_g est registrée en fonction de la charge de grille Q_g. De la courbe V_g–Q_g il est possible de déterminer directement la caractéristique ϕ_s–Q_g.

Parce que la charge dans l'intérieur du silicium sous l'oxyde de grille $Q_s(\phi_s)$ est connue de la littérature on peut déterminer facilement la charge d'états de surface en fonction de ϕ_s. La méthode est appliquée aux quelques transistors MOS à substrat *n* et *p*. Aussi on discute la précision de la méthode proposée et on fait une comparaison avec des méthodes existantes. De cette comparaison on peut conclure que la méthode proposée est attractive par sa simplicité.

Zusammenfassung – Eine einfache Methode zur Ladungsmessung in Oberflächenzuständen als Funktion des Oberflächenpotentials in MOS Transistoren und MOS Kondensatoren wird vorgeschlagen.

Ein konstanter Gleichstrom wird der Steuerelektrode eines MOS Transistors zugeführt. Mittels eines Operationsverstärkers wird die Steuerspannung V_g bezogen auf den Substrat, als Funktion der Steuerelektrodenladung Q_g geschrieben. Die Steuerelektrodenladung als Funktion des Oberflächenpotentials ϕ_s kann direkt aus der V_g–Q_g Kennlinie abgelesen werden.

Da die Siliziumladung $Q_s(\phi_s)$ aus der Literatur bekannt ist, kann die Oberflächenzustandsladung leicht als Funktion von ϕ_s bestimmt werden. Die Methode wird durch Messungen an MOS Transistoren vom *n*- und *p*-Typ verdeutlicht. Schlieszlich wird die Genauigkeit der Ladungsmessungsmethode diskutiert und mit anderen Methoden zur Bestimmung der Oberflächenladung verglichen. Hieraus ergibt sich als Vorzug der Ladungsmessungsmethode, ihre grosze Einfachheit.

INTRODUCTION

THE DETERMINATION of the charge distribution at the Si–SiO_2 interface in MOS capacitors or transistors has been the subject of a number of papers [1–14]. Knowledge of the charge distribution, and more precisely, knowledge about the charge in the so-called 'interface states' is of value for those who are concerned about the electrical performance of MOS capacitors and transistors.

The method most employed for a determination of the charge distribution is based upon a differential capacitance measurement on the MOS system under varying d.c. bias. This method, as well as its interpretation, has been discussed extensively [2–9]. In this paper we intend to present an alternative charge measuring method, which is based upon the direct measurement of charge supplied to the MOS system as a function of bias. One of the advantages of the method is its physical clearness.

THE CHARGE MEASURING METHOD

In Fig. 1(a) we have depicted a parallel plate condenser, being charged by a current I_0. When we plot (Fig. 1(b)) the capacitor voltage V_g vs. the plate charge Q_g, we find a straight line with slope C_0^{-1} if C_0 is the capacitance of the condenser. In the case that the two metal plates are similar and their work functions equal, the straight line in Fig. 1(b) will pass through the origin. However, when the work function difference between top plate and bottom plate $\Phi_1 - \Phi_2 = \Phi_{12}$ is finite, the plate charge will just be zero when V_g is equal to the contact potential $\phi_{12} = -q^{-1}\Phi_{12}$. In general the capacitor voltage V_g satisfies:

$$V_g = \phi_{12} + Q_g \cdot C_0^{-1} \tag{1}$$

We take a step further by assuming that the bottom plate of the condenser in Fig. 1(a) is replaced by a piece of silicon. The top plate is equivalent to the 'gate' and between gate and silicon a dielectric medium like SiO_2 is present. Now we must remember that, unlike the case for the metal plate condenser a potential will develop in the silicon over a finite distance, if surface charge is applied. If ϕ_s is the potential at the silicon surface with respect to its interior, we can write down the following relationship between gate voltage V_g and gate charge Q_g:

$$V_g = \phi_{MS} + Q_g \cdot C_0^{-1} + \phi_s \tag{2}$$

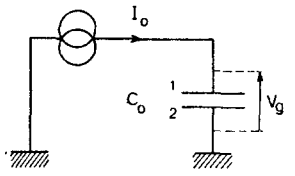

Fig. 1(a). A parallel plate condenser, charged by a constant d.c. current.

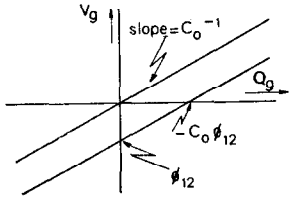

Fig. 1(b). The voltage V_g as a function of the plate charge Q_g across the capacitor C_0 in Fig. 1(a).

ϕ_{MS} denotes the contact potential between gate metal and silicon. Equation (2) expresses that for the MOS system V_g as a function of Q_g behaves very much like in the case of a parallel metal plate condenser, except that a displacement ϕ_s along the V_g axis, which is dependent on Q_g, has to be accounted for.

Under the condition of strong surface accumulation ($V_g \gg 0$ for n-type and $V_g \ll 0$ for p-type silicon) or strong surface inversion ($V_g \ll 0$ for n-type and $V_g \gg 0$ for p-type silicon), ϕ_s attains a more or less constant value and the slope of V_g vs. Q_g tends to C_0^{-1} (Fig. 2).

There is an intermediate region, where ϕ_s changes from its minimum to its maximum value.

Assuming that the value of the surfacepotential ϕ_s in point A is known (Fig. 2) lines of equal and known surfacepotential can be drawn in the measured V_g–Q_g plot. According to expression (2) all these lines should have a slope C_0^{-1}. From the intersections of the equi-surfacepotential lines with the V_g–Q_g plots, Q_g and V_g can be determined as a function of ϕ_s.

We now have a closer look at Q_g, the plate charge. For reasons of neutrality Q_g should be compensated by a charge $-Q_g$ on the silicon side, which consists of four components:

- depletion charge of ionized bulk impurities
- excess charge carriers in the silicon, near the interface
- charge Q_{ss} in interface states, which interacts with charge carriers in the silicon
- constant charge Q_0 in the dielectric medium, which is assumed to be located near the interface.

When the charge inside the silicon – the sum of the two first contributions – is denoted by Q_s, we may write:

$$Q_g = -(Q_s + Q_{ss} + Q_0) \tag{3}$$

Provided that the silicon doping level is known and conditions of thermal equilibrium exist, the silicon charge Q_s is known as a function of ϕ_s[1, 15]. Substitution of $Q_g(\phi_s)$ and $Q_s(\phi_s)$ into (3) yields $Q_{ss} + Q_0$ as a function of the surfacepotential ϕ_s, which is the main objective of our paper.

So far we have indicated how, in principle, from the measurement of gate voltage vs. gate charge on an MOS system, information can be obtained about the interface state charge density as a function of surfacepotential.

Before we proceed to a description of the actual measurement set-up and the charge measurements, we have still to explain in detail how essential parameters like oxide capacitance C_0 and the surfacepotential ϕ_s are determined and how they can be used for a detailed interpretation of measured V_g–Q_g plots.

THE EVALUATION OF GATE VOLTAGE VS. GATE CHARGE PLOTS

This section treats the determination of the surface potential ϕ_s as a function of V_g from an analysis of the V_g vs. Q_g plot.

In the condition of very strong accumulation or very strong inversion the silicon charge will be dominated by excess charge carriers near the interface and equation[3] reduces to $Q_g \approx -Q_s$. Theoretical considerations[1, 15] lead to the following expressions for the silicon charge:

$$\left.\begin{array}{l}\text{bulk: } p\text{-type}\\ \text{inversion } (\phi_s \gg 0)\\ Q_s = -qLn_i\left(\dfrac{n_i}{C_B}\right)^{1/2}\exp\left(\dfrac{q\phi_s}{2kT}\right);\\ \text{bulk: } n\text{-type}\\ \text{inversion } (\phi_s \ll 0)\\ Q_s = +qLn_i\left(\dfrac{n_i}{C_B}\right)^{1/2}\exp\left(\dfrac{-q\phi_s}{2kT}\right);\end{array}\right\} \qquad \left.\begin{array}{l}\text{accumulation } (\phi_s \ll 0)\\ Q_s = +qLn_i\left(\dfrac{C_B}{n_i}\right)^{1/2}\exp\left(\dfrac{-q\phi_s}{2kT}\right)\\ \text{accumulation } (\phi_s \gg 0)\\ Q_s = -qLn_i\left(\dfrac{C_B}{n_i}\right)^{1/2}\exp\left(\dfrac{q\phi_s}{2kT}\right)\end{array}\right\} \quad (4)$$

In these expressions n_i is the intrinsic concentration ($1{\cdot}5\times10^{10}\,\text{cm}^{-3}$; 300°K); L is the Debye–Hückel length: $(2\epsilon_{si}kT/qn_i)^{1/2} = 4.8\times10^{-3}$ cm at 300°K; $(kT/q) = 26{\cdot}10^{-3}$ V at 300°K; ϵ_{si} is the permittivity of silicon and C_B is the bulk dope concentration.

In Fig. 3(a) V_g vs. Q_g plot, measured on an n-type bulk MOS transistor is shown. When we consider two points A and B on this plot equally far into inversion and accumulation and we assume that for these points $Q_g = -Q_s$ is given by expressions (4) and furthermore that $|Q_{s,A}| = |Q_{s,B}|$ then we can derive:

$$|\phi_{s,A} - \phi_{s,B}| = \frac{4kT}{q}\ln\frac{|Q_{s,A\text{ or }B}|}{qLn_i} \qquad (5)$$

$$\frac{\phi_{s,A}+\phi_{s,B}}{2} = -\frac{kT}{q}\ln\frac{C_B}{n_i} \qquad (6)$$

Equation (5) yields the range of ϕ_s values covered by the V_g–Q_g measurement between A and B. It is apparent from (5) that this range is independent of the bulk dope C_B. Figure 4 shows a plot of computed $|\phi_{s,A} - \phi_{s,B}|$ values as a function of $Q_{s,A\text{ or }B}$. Equation (6) indicates that the average surfacepotential is the potential for which the surface becomes intrinsic. The average surfacepotential as a function of dope concentration C_B is shown in Fig. 5.

With the aid of the above knowledge we can again analyse the V_g–Q_g plot. According to expression (2) in point A of Fig. 3:

$$V_{g,A} = \phi_{MS} + Q_{g,A}\,.\,C_0^{-1} + \phi_{s,A}$$

We can now obtain from Fig. 4 the surfacepotential interval $|\phi_{s,A} - \phi_{s,B}|$ associated with the charge $|Q_{s,A}|$. When in point A a vertical line segment of length $|\phi_{s,A} - \phi_{s,B}|$ is drawn, the top A' of this segment will represent a gate voltage:

$$V_{g,A'} = \phi_{MS} + Q_{g,A}\,.\,C_0^{-1} + \phi_{s,B}$$

In point B the gate voltage obeys:

$$V_{g,B} = \phi_{MS} + Q_{g,B}\,.\,C_0^{-1} + \phi_{s,B}$$

or by subtraction we find:

$$C_0 = \frac{Q_{g,B} - Q_{g,A}}{V_{g,B} - V_{g,A'}} \qquad (7)$$

The construction of Fig. 3, based on expression (7) allows us to determine C_0. It also furnishes the means to construct the equi-surfacepotential lines, as we have described in the preceeding sections by drawing straight lines parallel to A'/B. It should

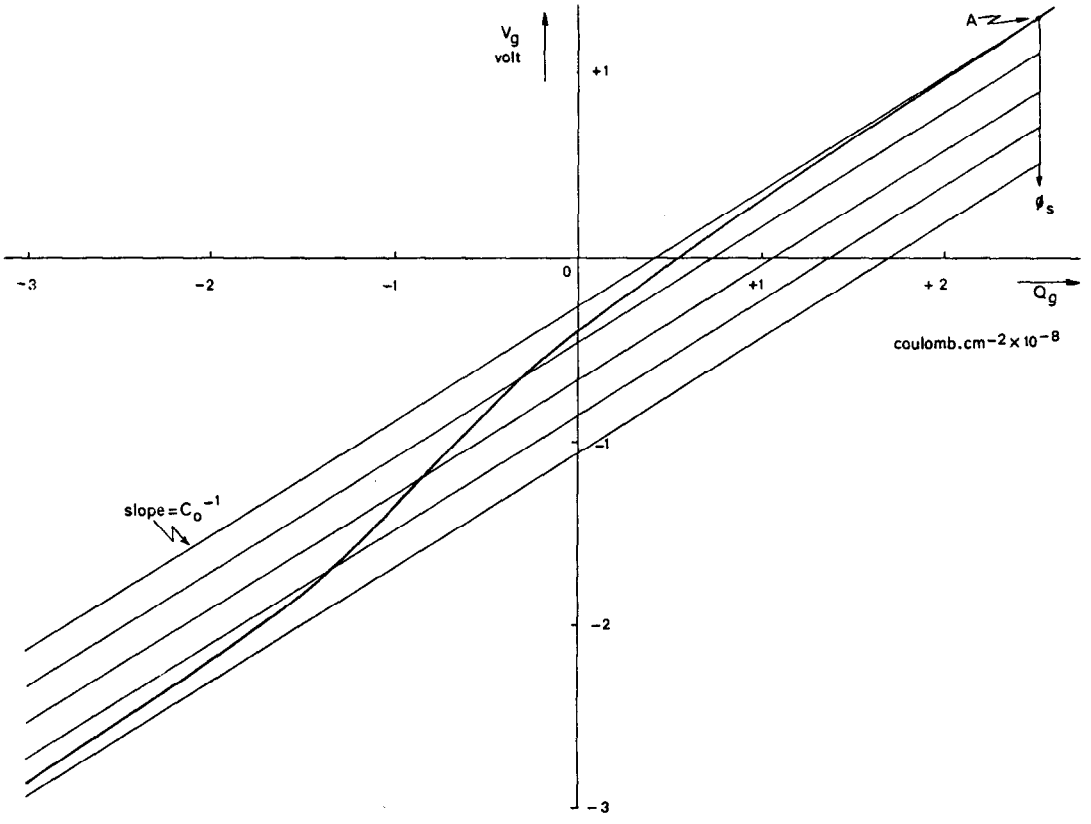

Fig. 2. The gate voltage V_g as a function of the gate charge Q_g for an n-type MOS transistor (sample 2, listed in Table 1).

be clear that due to expression (6) the equi-surfacepotential line which crosses AA' half way is the 'intrinsic' surface line. When the potential associated with this line is known from an evaluation of (6), the potentials associated with all other lines are also known.

An equi-surfacepotential line of special importance is the line $\phi_s = 0$ which according to (2) crosses the V_g axis in $V_g = \phi_{MS}$ (Fig. 6). The intersection between the line $\phi_s = 0$ and the V_g-Q_g plot indicates the 'flat-band' situation where $Q_s = 0$.

A prerequisite for the derivation of the surface potential ϕ_s of the equi-surfacepotential lines is the existence of two points A and B on the V_g-Q_g plot, equally far into inversion and accumulation, where the silicon charge should be dominated by charge carriers and the two values of the charges should be equal. Inevitably the determination of the location of A and B will be subject to inaccuracy. Errors in the estimate of $Q_{g,A}$ and $Q_{g,B}$ of the order of 20 per cent will however, due to the logarithmic nature of expression (5) lead to an error of about 10 mV in the determination of $|\phi_{s,A} - \phi_{s,B}|$ which is usually negligible.

THE MEASUREMENT APPARATUS

The principle of the measurement is shown in Fig. 7(a). A constant charging current I is fed into the inverting input of an operational amplifier, connected to the bulk electrode of an MOS transistor. The bulk electrode has been shorted to the drain and source electrodes. The gate of the MOS transistor is connected to the output of the operational amplifier and an xy-recorder, on which V_g is plotted vs. time.

As the rate of change of the charge flowing into the gate is constant the recording of V_g vs. time will be equivalent to a recording of V_g vs. the charge Q_g.

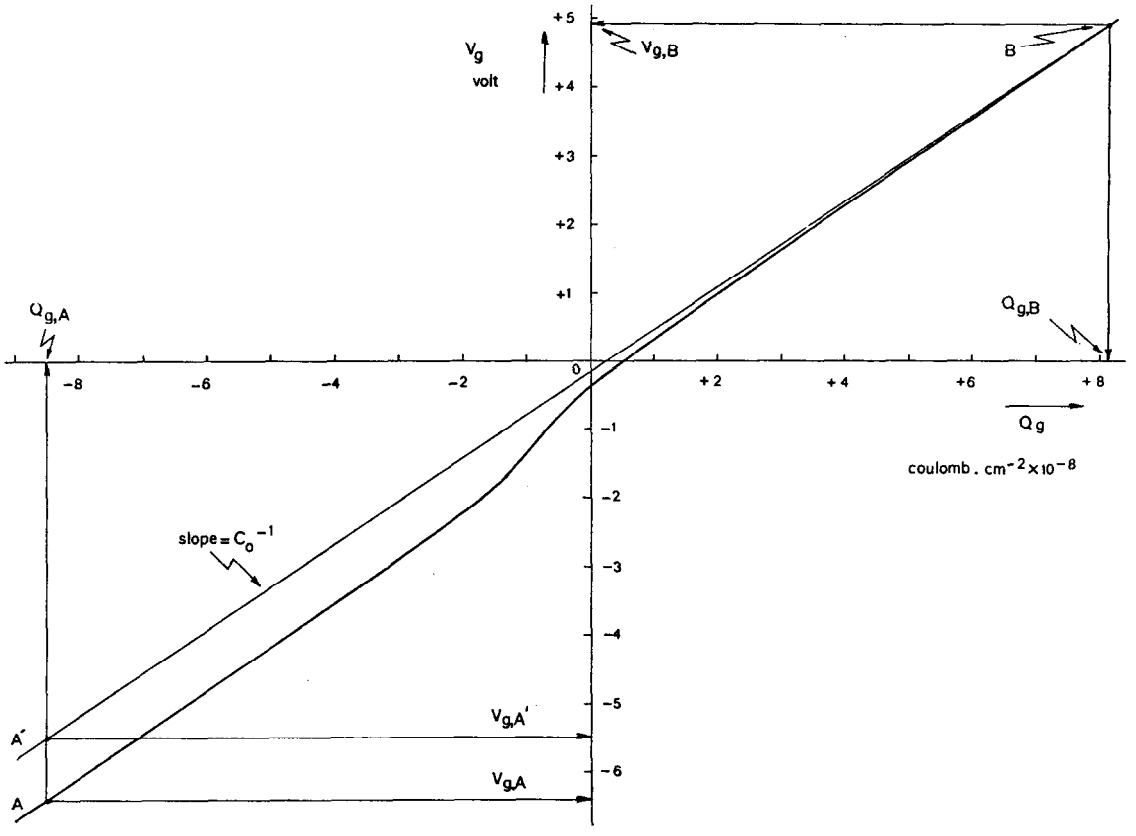

Fig. 3. The gate voltage V_g as a function of the gate charge Q_g for the same MOS transistor as in Fig. 2.

The battery in the gate circuit is needed to adjust the startpoint of the V_g–Q_g plot.

In practice the current source I and the operational amplifier in Fig. 7(a) are provided by the Keithley solid state electrometer model 602, used in the 'Ohmmeter operation' condition. The electrometer is connected as illustrated in Fig. 7(b). It is used as an operational amplifier with terminals J101 and J102 as the differential input. The terminal J106 acts as the inverting output and controls the gate voltage V_g of the MOS transistor. The current source I is provided within the

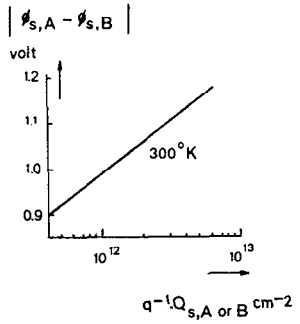

Fig. 4. The computed values $|\phi_{s,A} - \phi_{s,B}|$ as a function of $q^{-1}Q_{s,A \text{ or } B}$.

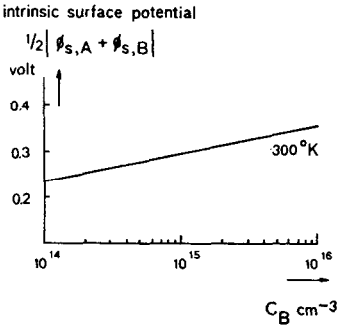

Fig. 5. The intrinsic surfacepotential $\frac{1}{2}|\phi_{s,A} + \phi_{s,B}|$ as a function of the bulk dope density C_B.

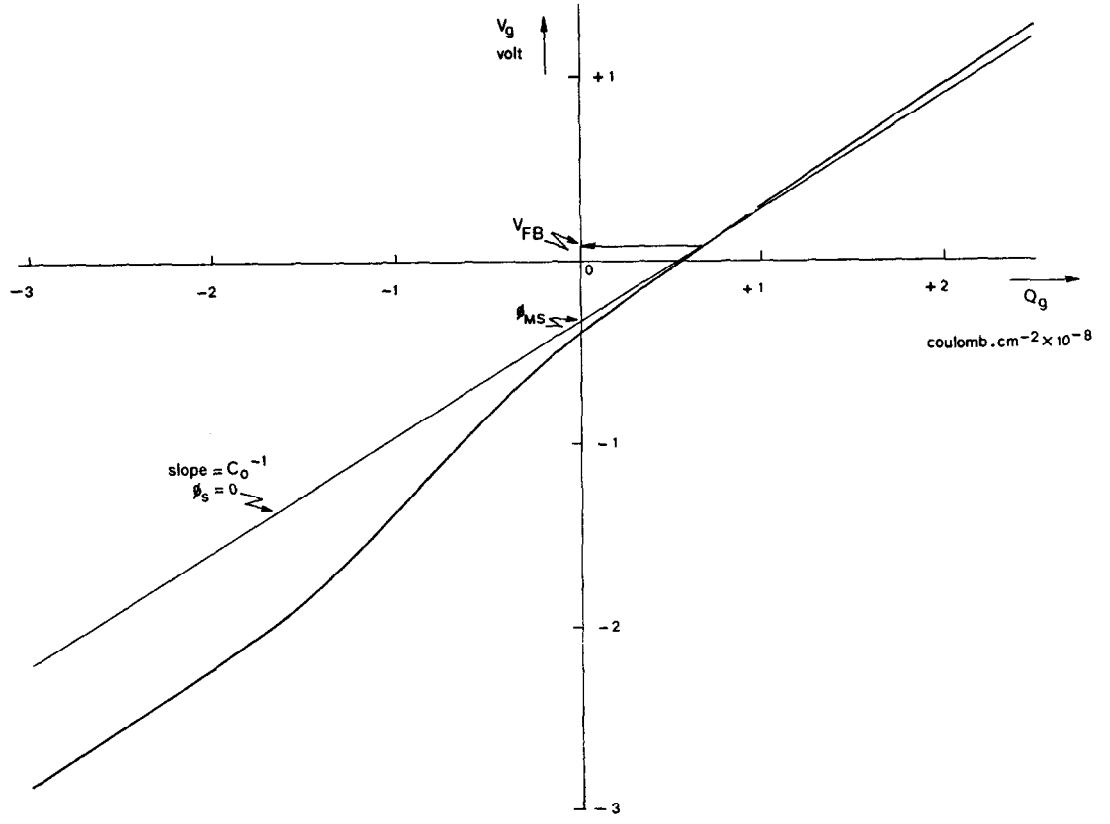

Fig. 6. The gate voltage V_g as a function of the gate charge Q_g for the same MOS transistor as in Fig. 2.

electrometer between the terminals J101 and J102 and may be chosen between the values 10^{-12} and 10^{-5}A. The zero switch allows short circuiting of the terminals J101 and J102. With the zero switch shorted the voltage supply A can be adjusted for the desired startpoint of the V_g-Q_g plot.

Typical values for the gate current density in the charge measuring method should lie between 10^{-10}-10^{-9} A cm^{-2} sec^{-1}.

In our measurements shown in Fig. 9 the current

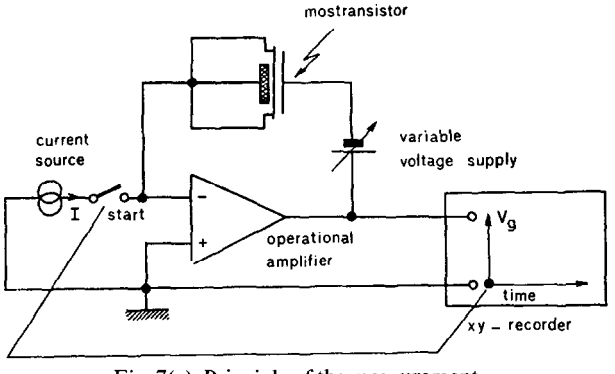

Fig. 7(a). Principle of the measurement.

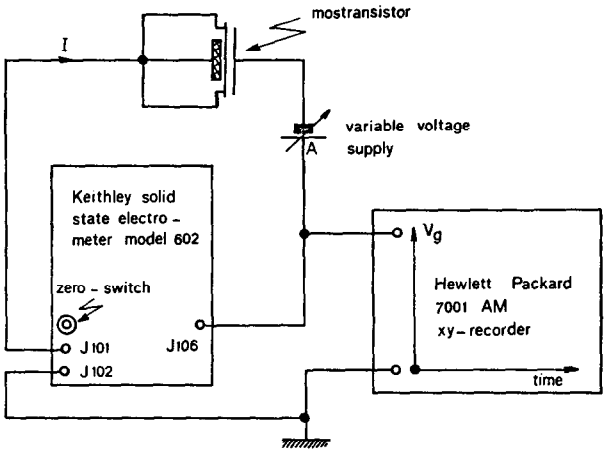

Fig. 7(b). The measurement apparatus.

source was set at 10^{-11} A. The oxide capacitances C_0 of the samples 1, 2 and 3 of Table 1 were 300, 180 and 180 pF respectively.

ILLUSTRATION OF THE USE OF THE CHARGE MEASURING METHOD

The method will be domonstrated on the following samples: an MOS transistor with relatively many surface states (sample 1) and two MOS transistors with relatively few surface states (the samples 2 and 3). The characteristics of the MOS transistors have been listed in Table 1. All the MOS transistors have the same geometry, represented in Fig. 8.

The total charge storage in the silicon and at the Si-SiO_2 interface $Q_0+Q_{ss}+Q_s$ of these samples has been graphically determined as a function of ϕ_s by the methods of the preceeding sections and the results are given in Figs. 9(a), (b) and (c). In the same figures the charge Q_s inside the silicon has also been plotted as a function of ϕ_s. $Q_s(\phi_s)$ was obtained from curves published by Whelan [15].

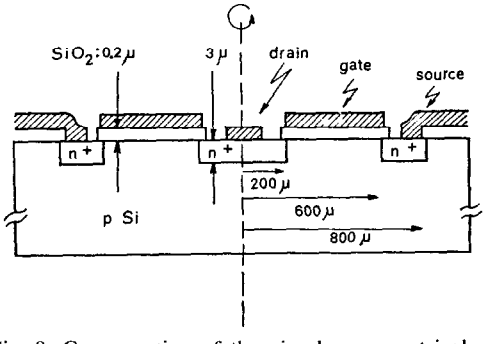

Fig. 8. Cross-section of the circular symmetrical MOS transistor used for the measurements.

The bulk dope C_B has been determined by two independent measurements:

1. The measurement of the small signal capacitance between the bulk electrode and the shorted source and drain electrodes as a function of gate bias, yielding the high frequency silicon space charge capacitance $C_{Si,\,min}$ under the condition of inversion. The relation between $C_{Si,\,min}$ and the bulk dope C_B is given in [15].
2. A measurement of the influence of substrate bias upon the channel conduction of the MOS transistor, yielding the bulk dope C_B in the condition of surface inversion [16].

The dope values determined by these methods have been presented in Table 1 and were found to be equal within experimental error. The value of the contact potential ϕ_{MS} has been taken from the literature [17].

The oxide capacitances C_0 obtained from the construction of Fig. 3 have been compared with the results of small signal capacitance measurements of C_0 (10 Khz) and were found to be equal. So there have been no serious leakage or polarization currents through the oxide during the charge measurements. By a subtraction of the charge inside the silicon Q_s from the total charge $Q_0+Q_s+Q_{ss}$, the charge storage in surface states Q_0+Q_{ss} as a function of ϕ_s is determined and represented in Figs. 10(a), (b) and (c).

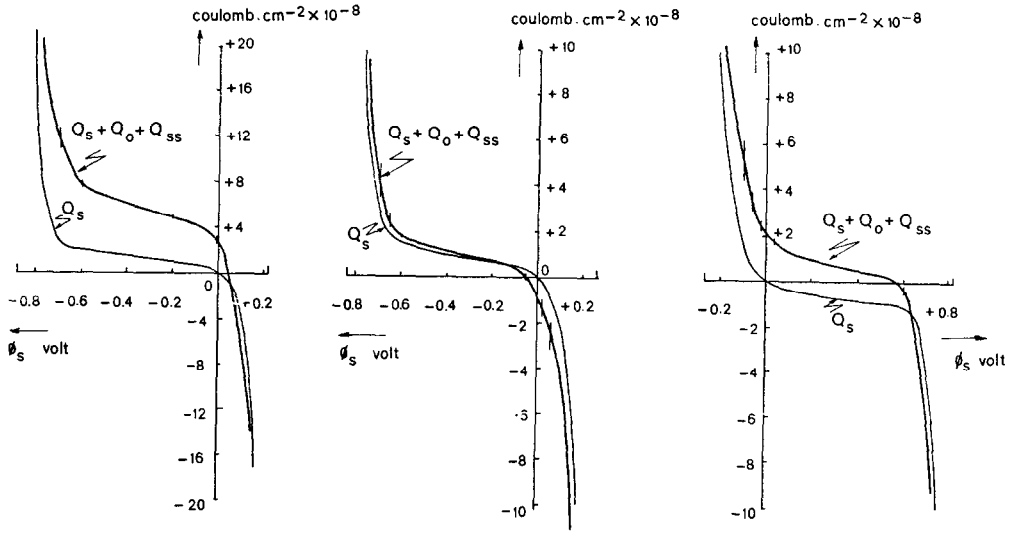

Fig. 9(a), (b) and (c). The charges $Q_0 + Q_{ss} + Q_s$ and Q_s as a function of ϕ_s for the samples 1, 2 and 3 respectively.

Table 1. Characteristics of the MOS transistors used for the measurements

Sample number*	1	2	3
Type of silicon	*n*	*n*	*p*
Surface orientation	1.1.1.	1.0.0.	1.0.0.
Donor or acceptor concentration of bulk Si			
Determined by method 1	$1{\cdot}8 \times 10^{15}$	8×10^{14}	$5{\cdot}6 \times 10^{14}$
Determined by method 2	$1{\cdot}8 \times 10^{15}$	8×10^{14}	$6{\cdot}7 \times 10^{14}$
Thickness of the insulator (Å)	1200	2000	2000
Structure of the insulator	SiO_2 Oxide dry grown at 1150°C	SiO_2–P_2O_5 Oxide dry grown at 1200°C Thickness of P_2O_5 glass layer: 300 à 400 Å	
Heat treatment to remove surface states	No heat treatment	Heat treatment: 450°C–N_2; 80°C–H_2O during 30′	
Gate metal	Al	Al	Al

*Samples 1 and 3 were manufactured at Philips Research Laboratories, Eindhoven, Netherlands and were obtained from Mr. M. V. Whelan. Sample 2 was prepared in our laboratory by Mr. J. Holleman.

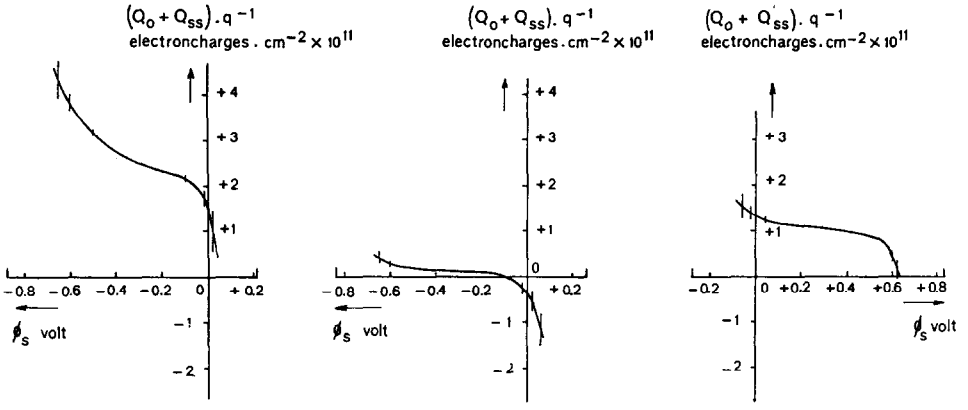

Fig. 10(a), (b) and (c). The charge Q_0+Q_{ss} as a function of ϕ_s for the samples 1, 2 and 3 respectively.

From Figs. 10(a), (b) and (c) we conclude that the rate of change of charge storage in surface states is relatively small for ϕ_s values in the intrinsic region of the silicon surface and relatively large for ϕ_s values in the regions near the valence band and conduction band edge of the surface of the semiconductor. This behaviour of charge storage in surface states has also been observed by other authors [8, 12, 13] using different techniques for the investigation of the Si–SiO_2 interface.

The curves of Figs. 9 and 10 serve as examples of the charge measuring technique. In samples 2 and 3 different values of oxide charge Q_0+Q_{ss} were found although the preparation of the samples was identical, according to Table 1. Because the samples 2 and 3 were prepared at different laboratories (see footnote Table 1), we attribute these variations in Q_0+Q_{ss} to other differing factors in the manufacturing processes by which samples 2 and 3 were obtained.

DISCUSSION OF THE ERRORS ARISING IN THE APPLICATION OF THE CHARGE MEASURING METHOD

An important condition for the interpretation of the V_g–Q_g plot is the existence of thermal equilibrium inside the silicon material and at the Si–SiO_2 interface. Actually the V_g–Q_g plot is measured under non-equilibrium conditions because during the measurement the charges in the silicon and at the Si–SiO_2 interface $Q_0+Q_{ss}+Q_s$ and in the gate Q_g change with time. In general the shape of the V_g–Q_g plot depends on the rate of change of gate charge dQ_g/dt during the measurement of the V_g–Q_g plot. However as found from the measurements for low values of dQ_g/dt ($10^{-10}-10^{-9}$ coulomb cm^{-2} sec^{-1}) the V_g–Q_g plot appeared to be independent of this rate. Hence we conclude that the V_g–Q_g plots have been measured under the condition of quasi-thermal equilibrium.

The estimated error in the determination of C_0 by the construction of Fig. 3 was less than 1 per cent. Also the error in the intrinsic surfacepotential $\Delta\phi_{s,\ \text{intrinsic}}$ was estimated at $\frac{1}{2}kT/q$ V. These two errors together determine the error $\Delta(Q_0+Q_{ss}+Q_s)$ in the $Q_0+Q_{ss}+Q_s$ vs. ϕ_s plots of Figs. 9(a), (b) and (c). For the error $\Delta(Q_0+Q_{ss}+Q_s)$ as a function of ϕ_s the following expressions can be derived:

$$|\Delta(Q_0+Q_{ss}+Q_s)| = \frac{|\Delta Q_g|}{\Delta\phi_s}\cdot\Delta\phi_s \qquad (8)$$

where

$$|\Delta\phi_s| < \left|\Delta\phi_{s,\ \text{intrinsic}} + \frac{\Delta C_0}{C_0}\frac{|Q_g - Q_{g,\ \text{intrinsic}}|}{C_0}\right| \text{ and}$$

$$\frac{|\Delta Q_g|}{\Delta\phi_s} = \frac{\Delta Q_g}{\Delta V_g}\frac{1}{|1-(\Delta Q_g/C_0\Delta V_g)|}$$

The maximum error $\Delta(Q_0+Q_{ss}+Q_s)$ has been computed by applying (8) to various points of the curves of Figs. 9(a), (b) and (c) and its magnitude has been indicated by small vertical lines in Figs. 9(a), (b) and (c).

The error $\Delta(Q_0+Q_{ss})$ in the Q_0+Q_{ss} vs. ϕ_s plots of Fig. 10 is determined by the error in the surfacepotential $\Delta\phi_s$ mentioned before and the error in the determination of the bulk dope density C_B (20 per cent). This maximum error $\Delta(Q_0+Q_{ss})$ is estimated for various points of the curves of

Figs. 10(a), (b) and (c) and its estimated magnitude has also been indicated by small vertical lines in Figs. 10(a), (b) and (c).

COMPARISON OF THE CHARGE MEASURING METHOD WITH OTHER TECHNIQUES FOR INVESTIGATING THE Si–SiO_2 INTERFACE

The charge measuring method is an alternative method for the investigation of the Si–SiO_2 interface. This method resembles in a way the low frequency thermal equilibrium C–V measurement method of Berglund[9]. Therefore we shall compare these two methods first.

Both methods yield the surface charge as a function of surfacepotential; in Berglund's method from an analysis of the derivative of the surface charge vs. surfacepotential $d(Q_{ss}+Q_s)/d\phi_s$ and in the charge measuring method from a direct analysis of the V_g–Q_g plot. One of the advantages of the charge measuring method is that information about the fixed oxide charge Q_0 is not 'lost'. On the other hand Berglund's method will be more sensitive for a variation of surface state charge density as a function of surfacepotential as it measures incremental charge rather than total charge.

In both methods the relationship between the measured gate voltage V_g and the actual surfacepotential ϕ_s should be established. In the C–V method an integration step is required and in the charge measuring method the relationship can be read directly from the V_g–Q_g plot. Also in both methods a 'matchpoint' is needed to link quantitatively the surfacepotential ϕ_s and the voltage V_g. We are of the opinion that the use of the intrinsic condition as a matchpoint has advantages over the use of the accumulation condition as a matchpoint, as done by Berglund. In the C–V method, especially if this method is employed on MOS transistors, the procedure for finding the intrinsic point may be based upon the procedure applied in the charge measuring method that we hope to outline in a forthcoming publication.

It should be admitted that the V_g–Q_g plot can also be obtained by electronically integrating a very low frequency C–V plot. We have not looked into this possibility, which in principle yields the same information, but which requires more complex instrumentation.

When we compare the charge measuring method with the high frequency C–V measurement method we notice similar differences as with the low frequency C–V method due to the incremental nature of C–V measurements.

Furthermore the range of surfacepotentials attainable with the charge measuring method will generally be larger and the influence of bulk series resistance will be negligible.

In conclusion we believe that the measurement of gate voltage vs. gate charge constitutes a lucid and easy-to-instrument method to obtain information about charge at the Si–SiO_2 interface.

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REFERENCES

1. C. G. B. Garrett and W. H. Brattain, *Phys. Rev.* **99**, 376, (1955).
2. R. Lindner, *Bell Syst. tech. J.* **41**, 803, (1962).
3. L. M. Terman, *Solid-St. Electron.* **5**, 285, (1962).
4. K. Lehovec, A. Slobodskoy and J. L. Sprague, *Phys. Stat. Sol* **3**, 447, (1963).
5. F. P. Heiman and G. Warfield, *IEEE Trans. Electron Devices*, **ED-12**, 167, (1965).
6. K. H. Zaininger and G. Warfield, *IEEE Trans. Electron Devices*, **ED-12**, 179, (1965).
7. A. S. Grove, B. E. Deal, E. H. Snow and C. T. Sah, *Solid-St. Electron.* **8**, 145, (1965).
8. M. V. Whelan, *Philips Res. Rep.* **20**, 562, (1965).
9. C. N. Berglund, *IEEE Trans. Electron Devices*, **ED-13**, 701, (1966).
10. P. V. Gray and D. M. Brown, *App. Phys. Letters*, **8**, 31, (1966).
11. E. H. Nicollian and A. Goetzberger, *Appl Phys. Letters*, **10**, 60, (1967).
12. E. H. Nicollian and A. Goetzberger, *Bell Syst. tech. J.* **46**, 1055, (1967).
13. E. Arnold, *IEEE Trans. Electron Devices*, **ED-15**, 1003, (1968).
14. M. Kuhn, *Recent News Paper, Electrochem. Soc. Conf.*, New York, May (1969).
15. M. V. Whelan, *Philips Res. Rep.* **20**, 620–632, (1965).
16. J. A. van Nielen and O. W. Memelink, *Philips Res. Rep.* **22**, 55–71, (1967).
17. A. S. Grove, *Physics and Technology of Semiconductor Devices*, John Wiley, New York, (1967).
18. D. R. Kerr, *M.I.S. Measurement techniques utilizing slow voltage ramps*, Presented at the conference on Properties and use of M.I.S. structures, Grenoble, France. 17–20 June (1969).