A Delay Spread Cancelling Waveform Characterizer for RF Power Amplifiers

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(Invited Paper)

***Abstract*—A two channel 65 nm CMOS RF-waveform characterizer is presented that enables multi-harmonic Adaptive Matching Networks (AMN) or Adaptive Digital Pre-Distortion (ADPD) in RF-power amplifiers. The characterizer measures the DC component and the first 3 harmonics of RF signals by applying a DFT to 8 (ideally) equally spaced quasi-DC output voltages. Conventionally in these types of systems accuracy is limited by sample timing accuracies, which in our case are mainly due to delay cell mismatch. We introduce a novel way to cancel delay cell mismatch, that significantly increases measurement accuracy at the cost of only a small power and area increase. The RF-waveform characterizer achieves 6.8-bit measurement linearity together with a (clock feedthrough limited) 24 dB SFDR. The measured power consumption for our proof-of-principle demonstrator is 18.6 mW at a maximum input signal frequency of 1.1 GHz under continuous operation.**

***Index Terms*—CMOS integrated circuits, Discrete Fourier transform, Signal sampling, Power amplifiers, Signal characterization, Delay spread cancellation**

I. Introduction

FULLY integrated RF-transceivers in advanced CMOS processes are common in many modern communication devices. In these, espacially RF-Power amplifiers (RF-PA) are affacted by Process-Voltage-Temperature (PVT) spread and source and load impedance mismatch. Both effects degrade RF-PA linearity and efficiency. Different handling conditions of the device can significantly change the antenna impedance [1], resulting in reflections that may damage the RF-PA. To compensate for these effects, Adaptive Digital Pre-distortion together with multi-harmonic adaptive matching networks and tunable bias networks can be used, where Adaptive matching networks can be efficiently designed [2]. Currently, implemented compensation techniques utilize temperature sensors, DC-sensors, power detectors [3] or peak detectors [4] to control bias networks or load impedance tuners to compensate for PVT spread and load impedance mismatch. However, with these techniques information about the shape of the RF-waveform is lost.

Proper control of Adaptive Digital Pre-distortion and multi-harmonic adaptive matching networks requires data on RF-PA linearity and impedances that can be derived from the harmonics of internal RF-waveforms. Here the 1^{st} harmonic contains information about e.g. impedance matching and output power. The 2^{nd} harmonic can be used to tune bias networks to improve efficiency and both the 2^{nd} and 3^{rd} harmonics can be used to improve linearity and to increase RF-PA efficiency [5] by using Adaptive Digital Pre-distortion and multi-harmonic adaptive matching networks.

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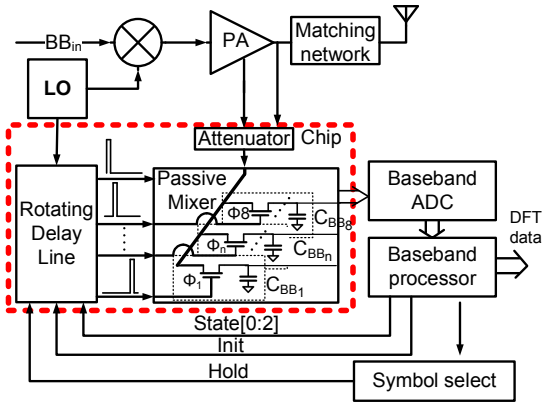

Fig. 1. Overview of the designed system; one out of two channels is shown for simplicity. The integrated part is depicted in the dotted box.

This work presents a 65nm CMOS RF-waveform characterizer that characterizes the DC value and the first 3 harmonic components of an input RF-waveform. The characterizer first mixes the RF-waveform using a N-path type mixer, after which a DFT yields the harmonic content of this waveform. For this type of sampling system, delay cell mismatch limits the accuracy of the waveform estimation. Our RF-waveform characterizer introduces a novel method to cancel the effects of this delay cell mismatch.

This brief first introduces in Section II the RF-waveform characterizer and the circuits used to sample the RF-waveform. In Section III the impact of delay errors on the performed DFT is discussed and a delay spread cancellation technique is introduced, that significantly increases the accuracy of the RF-waveform characterizer at the cost of only a modest power and area penalty. Section IV gives experimental results of the impact of the delay spread cancellation technique, followed by the conclusion in Section V.

II. Sampling Circuit

Any periodic waveform can be described by a Fourier sum of harmonic sinusoids, which are fully described by their phase, amplitude and frequency, where typically only the frequency of the first harmonic is known in transmit systems. Our RF waveform characterizer "samples" the RF-waveform period into a set of (ideally) equally spaced quasi-DC samples on which a DFT is applied to obtain the DC term and the amplitude and phase information of up to 3 harmonics. When sampling across a known impedance in series with the RF-PA

output, e.g. part of a matching network, the output power of the RF PA harmonics can be derived per harmonic allowing multi-harmonic tuning.

Fig. 1 shows the block schematic representation of one channel (for simplicity reasons) of the RF-waveform characterizer. It consists of a Delay Line (DL) locked to the RF-signal that creates 8 non-overlapping (ideally uniformly spaced) pulses over one period of the RF signal that drive the 8-phase passive mixer. The mixer downconverts the RF-waveform to quasi-DC voltages on capacitors C_{BBn}, after which the voltages at C_{BBn} are converted to the digital domain by a baseband ADC. Switching of the mixer upconverts the switch-C RC frequency domain behaviour to harmonics of the clock signal, resulting in only harmonics of the RF-signal being downconverted to baseband. The mixer bandwidth is given by $BW = D/f_{rc}$ [6] , where D is the duty-cycle of the mixer pulse and f_{rc} the RC bandwidth of the switch-C network. In our case D = 1/8 and $f_{rc} = 1/(2\pi\ 5k\Omega\ 10pF) \approx 3.2$ MHz resulting in $BW \approx 400$kHz, which is fast enough to characterize the effects of PVT spread. After sampling, the baseband processor applies an 8-point DFT to obtain the DC value and the first 3 harmonics of the RF input signal. A front-end 10x attenuator (9kΩ + 1kΩ in series) is used since the breakdown voltage of the used technology is 1.2V, while voltages in the RF PA can be significantly higher [7]. This attenuation prevents breakdown of the passive mixers and also limits the feedthrough of the passive mixer clock to the RF-input signal below -80 dBm.

Fig. 2 shows a more detailed schematic overview of one channel of the implemented circuit. It consists of a rotating delay line (see Section III), a pulse shaper and a switching matrix that ensures that the mixers sample the RF-signals on the correct baseband capacitors C_{BBn}. The pulse shaper converts the 50% duty cycle square wave to $\leq 12.5\%$ duty cycle pulse required to drive the 8-phase passive mixer, enabling the down-conversion of both even and odd harmonics. The large RC time constant in the mixer results in sinc-filtering of the downconverted RF-signal [6], which can easily be compensated for in the digital domain. Also, the passive mixer behaves like an N-path filter; hence the input impedance of the sampling system equals 18.85x R_{switch} of the mixer [8]. In our case the input impedance of the sampling system is about 100kΩ, therefore negligibly loading the attenuator.

III. Delay Spread Cancellation

A DFT assumes uniformly distributed sample points over a beat period, which in our demonstrator is the period of the first harmonic of the RF signal. However, delay cell mismatch causes static random mismatch between the sample points, resulting in delay errors Δt_{ϵ_N}(Fig. 3). In a locked delay line, the variance of the delay over the delay line [9] (Fig. 3) is given by:

$$\sigma_{\Delta_{tn}} = T_{Ref}^2 \frac{n(N-n)}{N^3} \sigma_{\epsilon n}^2 \qquad (1)$$

where $\sigma_{\Delta_{tn}}$ is the systematic mismatch after n cells, $\sigma_{\epsilon n}$ is the individual delay cell mismatch, N is the number of delay cells and n being the n-th output tap of the delay line. Both

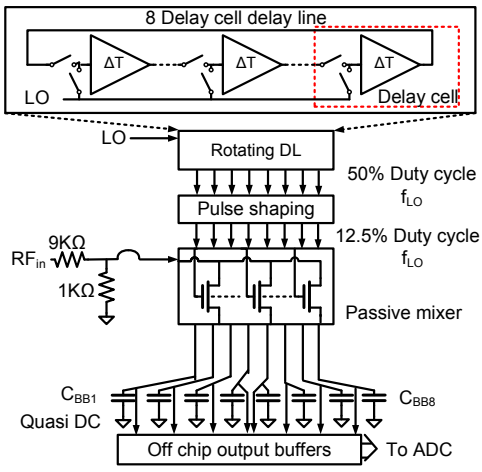

Fig. 2. Overview of the designed rotating delay line system.

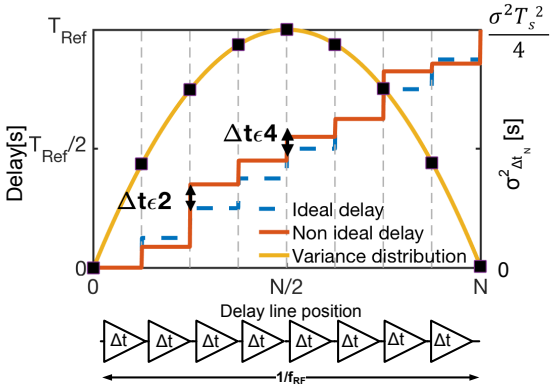

Fig. 3. Variance of the delay and delay distribution over the delay line for a standard DLL. N is the length of the delay line. Note that the variance of the delay over the line is zero at the begin and end of the line. This results in the average delay error being zero over the entire delay line when locked.

distribution are assumed to be normally distributed with a zero mean. The static random mismatch causes leakage between DFT bins in the DFT due to the ideal sampling moments becoming non-ideal, thereby reducing the dynamic range of the waveform estimation. Impedance level scaling (wider components in the delay cell and a proportional increase in power consumption) can alleviate mismatch-limited accuracy at the cost of area and power dissipation.

We implemented a power and area efficient method to ideally cancel the effect of delay spread in individual delay cells. This method is based on the statistical properties of mismatch having a zero mean (equation (2)), and properties of the variance in a Delay Locked Loop (DLL) as shown in equation (1).

$$\sum_{n=1}^{N} \Delta t_{\epsilon n} = 0 \qquad (2)$$

Cancellation of the impact of delay variations is implemented by rotating the N individual delay cells in the delay line in N steps, as shown in the top part of Fig. 4. Delay cell rotation is implemented by switches in front of all delay cells (see Fig. 2), that either connect the delay cell input to the previous delay cell or to the LO. For each of the N rotation states the

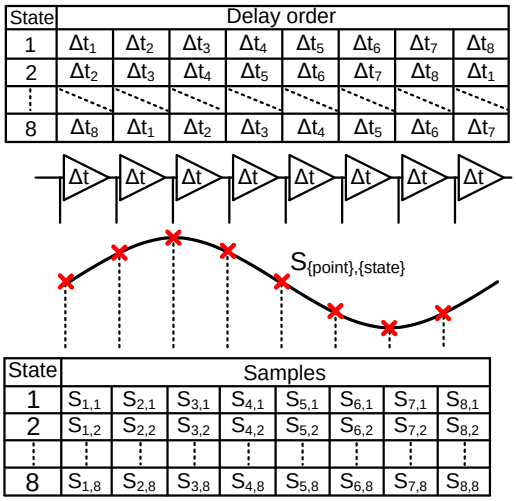

Fig. 4. Rotation order of the delay elements. Every delay element is used in every place in the delay line exactly once. During every rotation state the waveform is sampled, resulting in a N x N matrix, where N is the number of samples per period. In this work N=8. After one full rotation cycle is complete the results are averaged.

waveform is measured and after one full rotation there are N x N per-rotation-state measurements (as depicted in the bottom part of Fig. 4) and all delay cells have occupied every position exactly once. Then the average timing error at each position equals the average error of every delay cell, which is zero in a locked delay line. Consequently, digitally averaging the N per-rotation waveform measurements yields full cancellation of the delay cell spread at all sample time instances thereby vastly improving the accuracy of the waveform estimation without an area and power penalty. We call this technique Delay Spread Cancellation (DSC). Note that this is in contrast to Dynamic Element Matching, where due to mismatch shaping or mismatch scrambling, errors are effectively converted into noise [10].

DSC significantly improves the average sampling timing accuracy of the system, however after averaging of the voltage waveforms a residual error voltage waveform is still present. To illustrate the effect of DSC on this residual voltage error waveform we calculate the expected error signal power. First we calculate the Taylor expansion of a sine wave at a sample moment T_0 when we apply DSC:

$$\begin{aligned} f(t) =& \frac{1}{N}\sum_{n=0}^{N}\sum_{m=0}^{\infty}\frac{f^{(m)}(T_0)}{m!}(t-T_0)^m \\ =& \frac{1}{N}\sum_{n=0}^{N}\Bigg[f(T_0)+\frac{\partial f(T_0)}{\partial t}(t-T_0)+ \\ & \frac{1}{2}\frac{\partial^2 f(T_0)}{\partial t^2}(t-T_0)^2+\frac{1}{6}\frac{\partial^3 f(T_0)}{\partial t^3}(t-T_0)^3+\cdots\Bigg] \end{aligned} \tag{3}$$

where m denotes the m-th harmonic of the sampled signal. Now we use equation 3 to calculate the effect of the delay cell mismatch $\Delta t_{\epsilon n}$. Note that the zero order term

$$\frac{1}{N}\sum_{n=0}^{N} f(T_0) = f(T_0) \tag{4}$$

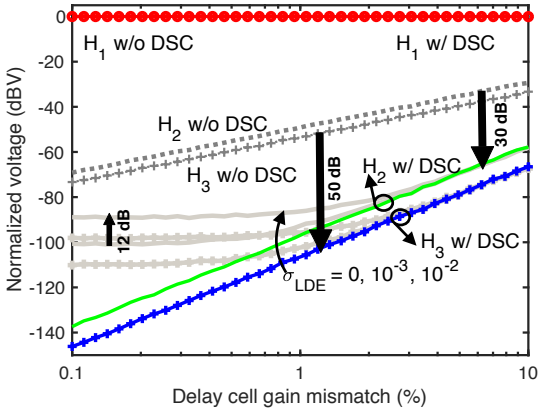

Fig. 5. Simulated effect of delay cell mismatch on leakage of H_1 into H_2 and H_3 in the DFT, assuming a sinusoidal input signal. The dotted lines are the results without DSC, where the solid lines without markers are the results after Delay Spread Cancellation (DSC) for H_2 for 3 different values of the layout dependent (relative) error to T_{Ref}, σ_{LDE}. The results for H_3 with DSC are the solid lines with + as marker.

is the ideal sample point. The effect of DSC is emphasized when we combine equation (2) and the first order term in equation (3) resulting in:

$$\frac{1}{N}\sum_{n=0}^{N}\frac{\partial f(T_0)}{\partial t}(\Delta t_{\epsilon n}-T_0)=0 \tag{5}$$

showing the cancellation of the error in first order. The dominant error is now given by the second order term in the Taylor expansion. Calculating the expected value for the error at sample moment T_0 we combine the second order term in equation (3) and equation (1) resulting in:

$$\begin{aligned} & E\Bigg[\frac{1}{2}\frac{\partial^2 f(T_0)}{\partial^2 t}\underbrace{\frac{1}{N}\sum_{n=0}^{N}(\Delta t_{\epsilon n}-T_0)^2}_{\sigma_n^2}\Bigg]= \\ & \frac{1}{2}\frac{\partial^2 f(T_0)}{\partial t^2}T_{Ref}^2\frac{n(N-n)}{N^3}\sigma_{\epsilon n}^2 \end{aligned} \tag{6}$$

Fig. 5 shows the simulation results of the effect of delay cell mismatch on the leakage of an ideal sinusoid to other bins in the DFT; here $H_1(\circ)$, $H_2(-)$ and $H_3(+)$ represent the 1^{st}, 2^{nd} respectively the 3^{rd} harmonic of the input signal. The dotted lines are w/o DSC, the solid lines are with DSC. A locked delay line was simulated with delay cells that have mismatch. The mismatch is modelled as a normally distributed gain error in the ideal delay of the delay cells as shown in equation (7), where Δt_n is the delay of the n^{th} delay cell, T_{ref} the reference period and σ_{e_n} the delay cell mismatch corresponding to the n^{th} delay cell.

$$\Delta t_n = \frac{T_{ref}}{N}(1+\sigma_{e_n}) \tag{7}$$

After adding mismatch the delay of all the cells is normalized so that the sum of all delays is equal to T_{ref}, after which the system is locked to the reference period. The sample instances of the locked delay line are now used to ideally sample a sinusoidal wave on which a DFT is performed. Fig. 5 shows the results of this simulation for both the conventional case and the case where delay spread cancellation is applied.

From Fig. 5 it can be concluded that the system with delay spread cancellation behaves like a second order system with a 40dB/decade slope, complying with equation (6). For a typical delay cell mismatch in our 65nm CMOS process of $\sigma_{\Delta tn} = 4.5\%$ a gain in dynamic range of 35 dB is observed.

Layout dependent matching and load matching errors impact the performance of the waveform characterizer, limiting the maximum dynamic range of the waveform characterizer. There are two types of layout dependent effects: in-loop and out of loop. Doubling the layout dependent effects in-loop (σ_{LDE}) decreases the DR by 12dB, due to the system being second order after rotation. Note that for the same reason, doubling the frequency for some matching level also decreases the DR by 12dB (see Fig. 5, light grey solid lines. H_2 has no markers, H_3 is marked with a +). σ_{LDE} is the standard deviation of the layout dependent time error relative to T_{Ref}. The out of loop error presents itself as deterministic sampling jitter comparable to that in ADCs.

IV. Measurement Results

A. System measurements

A demonstrator chip with a maximum input signal frequency of $f_0 = 1.1$ GHz and two channel input is designed to prove the principle of using the rotating delay line for the RF-waveform characterizer. The operating frequency is limited by the switches in front of the delay cell, the output buffer of the delay cell and the loading of the delay cell by the pulse shapers. Fig. 6 shows the photograph of the designed demonstrator chip. The two channel characterizer occupies a total active area of $0.11mm^2$ of which $0.05mm^2$ is occupied by the 16 capacitors. The overhead to implement the delay cell rotation is only 800 μm^2.The measurement setup consists of two signal generators (Agilent E8267D) to create the clock and RF-waveform signal, 8 SMUs (2x HP4156Bs') to digitize the capacitor voltages and a computer running MATLAB to only perform the averaging, an 8 point DFT, sync compensation and rotation. The SMUs could be replaced by a 10-bit ADC (to cover the full dynamic range of the RF-waveform characterizer). At the maximum RF signal input frequency of f_0 the power consumption equals 18.6 mW under continuous operation.

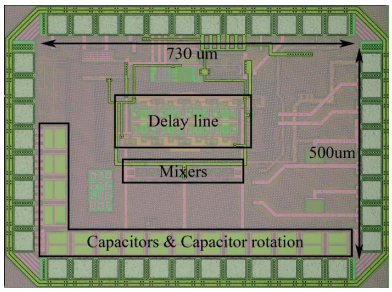

Fig. 6. Chip photo of the two channel waveform characterizer.

To demonstrate the performance of the RF-waveform characterizer, the harmonic spectrum of two power-combined signal generators is measured. This measurement mimics a PA during normal operation, where the measurements are performed before the matching network on internal signals of an integrated RF-PA. These internal signals before the matching network can contain significant harmonic content at the 2^{nd} and 3^{rd} harmonic. The output power of the first harmonic should remain constant during normal operation and the spurious emissions are measured and are to be reduced. The output of the first generator is a +10 dBm sine wave at frequency f_0. The power of the second sine wave generator is swept from -10 to 20 dBm at a frequency of $2{\cdot}f_0$ (Fig. 7) or $3{\cdot}f_0$ (Fig. 8) mimicking non-linearties in the RF-PA. The harmonics of the generators used for signal generation are well below the harmonics caused by non-linear effects in the RF-waveform characterizer. Fig. 7 and Fig. 8 show the three estimated harmonics of our system, as function of the 2^{nd} and 3^{rd} harmonic input power. In both graphs, the measured data per state is shown in grey, while the result after delay spread cancellation is shown in black. The highest improvement in accuracy is observed for low input powers as shown in Fig. 7, where the SNR of the 3^{rd} harmonic is improved by 20 dB by the introduced delay spread cancellation compared to using a conventional static delay line. The slope of the 3^{rd} harmonic in Fig. 7 is non-zero due to non-linear effects in the integrated mixer, where mixing of the 1^{st} harmonic with the

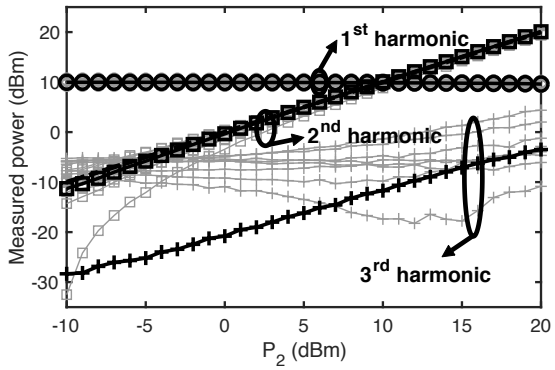

Fig. 7. Harmonic power spectrum for different values of P_{in2} at $2{\cdot}f_0$. P_{in1} = 10 dBm at f_0, P_{in3}= $-\infty$ dBm at $3{\cdot}f_0$. Ideal values are in dashed black lines, average over rotation states in solid black lines and per-rotation state values are in grey.

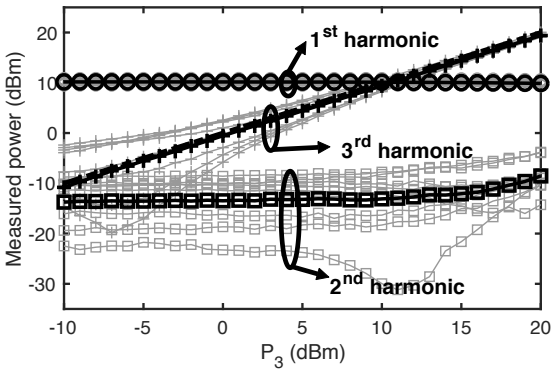

Fig. 8. Harmonic power spectrum for different values of P_{in3} at $3{\cdot}f_0$. P_{in1} = 10 dBm at f_0, P_{in2} = $-\infty$ dBm at $2{\cdot}f_0$. Ideal values are in dashed black lines, average over rotation states in solid black lines and per-rotation state values are in grey.

internal LO causes the static power level of the 2^{nd} harmonic in Fig. 8. The linearity of the RF-waveform characterizer is determined from the input power to output power slope. This slope is fitted with a polynomial function, where an ideal linear system only has a first order term. The second order term of the normalized polynomial function is the dominant non-linearity in the system and thus limits the overall linearity of the system. The second order terms of the two polynomial functions equals 0.0073 and 0.0094 for respectively the 2^{nd} and 3^{rd} harmonic power sweeps, resulting in a 7.1 and 6.7 bit linearity. In a similar way the linearity for the first harmonic is derived to be 6.8 bit. The SFDR is derived from Fig. 8, where the difference in power between the 1^{st} harmonic and the 2^{nd} harmonic is 24 dB. Extensive Spectre simulations show that clock feedthrough is the dominant limiting contribution for SFDR in our demonstrator chip.

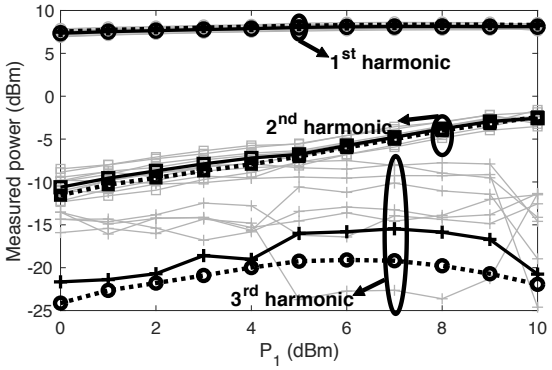

Fig. 9. Harmonic spectrum Mini-Circuits PA for different RF-PA input powers measured after the matching network with the designed system. Spectrum analyzer values are in dashed black lines, average over rotation states in solid black lines and per-rotation state values are in grey.

B. Measurements on a misbiased RF-PA

As next demonstration, the output of a Mini-Circuits ZX60-1215LN-S+ amplifier was measured. The amplifier is intentionally biased in such a way that it works far in compression. The input power of the 1^{st} harmonic to the Mini-Circuits amplifier is swept from 0 to 10 dBm at an operating frequency f_0 = 1.1GHz. The higher harmonics created by the generator are well below the harmonics generated by the Mini-Circuits amplifier under these conditions, therefor are not affecting the measurements. The output of the amplifier is measured both with the designed waveform characterizer system and using a spectrum analyzer (Agilent E4404B) for comparison. From Fig. 9 it can be concluded that the output power of the RF PA can be determined within 0.2 dB, 0.9 dB and 4 dB accuracy for respectively the 1^{st}, 2^{nd} and 3^{rd} harmonic with delay spread cancellation compared to 0.3 dB, 3 dB and 14.7 dB for the static delay line. The 1^{st} and 2^{nd} harmonics results of our RF-waveform characterizer after applying DSC are comparable to the results measured by the spectrum analyser. Especially for the 3^{rd} harmonic the accuracy of the measurement results is significantly increased by rotating the delay line and averaging the measurement results to achieve delay spread cancellation.

Comparing to [3], our work measures the phase and magnitude of the DC and first 3 harmonics of an RF-waveform instead of only derived parameters such as output power, DC current sensors and temperature sensors. This measured information about the RF-waveform shape allows ADPD. The total power consumption of the sensors in [3] is 18.4 mW, where our demonstrator consumes 18.6 mW.

V. Conclusion

We present a $0.11mm^2$ two-channel RF waveform characterizer to measure two RF-channels at about 6.8-bit accuracy, capturing e.g. the output and/or the internal signal of an RF-PA, thereby allowing ADPD and adaptive matching networks. We introduce delay spread cancellation as a power efficient module to significantly increase accuracy. By rotating the N delay elements inside the delay line exactly N times delay spread is fully cancelled, yielding on average ideal sample time instants. Applying DSC in a signal waveform sampler, the SNR of the measurement system increases by up to 20 dB without any significant increase in area ($800\mu m^2$) and power consumption (1mW). In our implementation, clock feedthrough limits its measurement accuracy. The system can easily be integrated with an RF-PA due to its relatively small size. The 6.8-bit linearity of the measurement system is maintained from -10 dBm to 20 dBm of RF input power at 1.1 GHz while consuming 18.6 mW (delay line, mixer and capacitor rotation for two channels) under continuous operation for our proof-of-principle demonstrator.

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